A Wideband RF Chipset for Multi-band Direct Conversion Transceivers

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Abstract

In a software-defined radio, the RF (Radio-Frequency) front-end must cope with multi-band radio signals. Therefore, we developed a wideband RF chipset for multi-band direct conversion transceivers. The chipset consists of a wideband quadrature mixer, a wideband low-noise variable-gain amplifier (LNVGA), and a multi-band local oscillator. The mixer achieves its wideband performance through the incorporation of newly developed power dividers. The LNVGA attains its wideband performance without the use of reactance elements. It also has high linearity due to a feedback circuit using two anti-series field-effect transistors. The local oscillator is able to cover the frequency bands of three systems, including a frequency-division duplexing system, while using only two voltage-controlled oscillators.

1. Introduction

There are currently various mobile communication standards in use worldwide. Software-defined radio (SDR) enables the creation of multi-standard terminals, which can be flexibly used in various mobile communication systems by simply rewriting their software [1]. However, to be compatible with different systems, the transceiver must be able to deal with various frequency bands. It is difficult to make transceivers with a superheterodyne architecture compatible with various systems, however, because such transceivers have IF (Intermediate-Frequency) channel filters and image-rejection filters that cannot be programmed to change the frequency band. In contrast, transceivers with a direct conversion architecture do not require IF-channel filters or image-rejection filters because they convert RF (Radio-Frequency) signals directly to baseband signals [2]. Thus, the direct conversion architecture is much more promising for designing a transceiver for SDR.

Transceiver components such as power dividers, phase shifters, local oscillators (LOs), and amplifiers must also be capable of wideband performance to cover the frequency bands of various systems. Although quadrature mixers using a 45º phase shifter for direct conversion transceivers have been reported [3], [4], there have been no reports of a 45º phase shifter that is compatible with wideband transceivers.

In this paper, we report on a wideband RF chipset for multi-band direct conversion transceivers that is compatible with three systems; the personal digital cellular (PDC), the PHS (Personal Handy-phone System) and the 2.4-GHz wireless LAN (WLAN). This chipset is based on a design that incorporates a quadrature mixer, a low-noise variable gain-amplifier (LNVGA), and a local oscillator [5]-[7]. We show that these components are suitable for frequency-widening applications in mobile transceivers and discuss the measurement results we obtained from MMICs (Monolithic Microwave Integrated Circuits) that we fabricated.

2. Transceiver configuration

Figure 1 shows a block diagram of the multi-band direct conversion transceiver. The same type of quadrature mixer was used for both the demodulator and the modulator. Therefore, they were able to share a local oscillator. The target systems were PDC, PHS,

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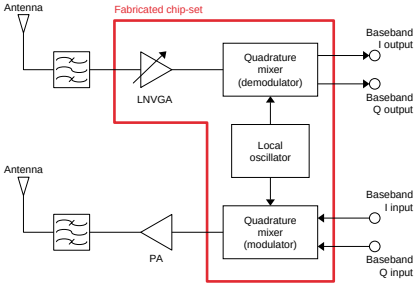


Fig. 1. Block diagram of the multi-band direct conversion transceiver.

and a 2.4-GHz WLAN. The first is an FDD (Frequency-Division Duplexing) system and the second and third are TDD (Time Division Duplexing) systems. Therefore, the target frequency range was from 0.9 to 2.5 GHz.

3. Quadrature mixer

The quadrature mixer consisted of two anti-parallel diode mixers, a 45° power divider, an in-phase power divider, and two differential amplifiers, as shown in Fig. 2. Use of the direct conversion architecture had two disadvantages: second-order distortion and DC offset. However, it was possible to eliminate them by using the anti-parallel diode mixers [8]. Such mixers, which connect diodes that have the same characteristics in parallel in reverse, do not output even-order signals. Consequently, the second-order distortion and DC offset equivalent to zero-order distortion were suppressed. Moreover, the anti-parallel diode

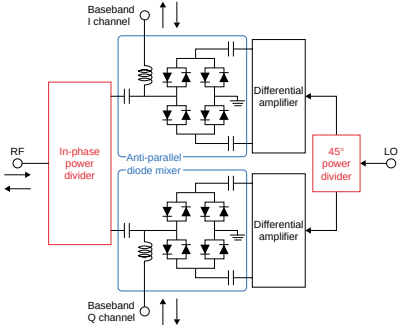


Fig. 2. Circuit configuration of the quadrature mixer.

mixers are even-harmonic mixers, which use LO signals whose frequency is half that of the RF signals. The mixers have a balanced configuration that enables them to obtain RF-to-LO isolation in a wide frequency range [9]. To generate in-phase and quadrature signals, we used a 45° phase shifter in the LO power divider. Our design targets for amplitude balance and quadrature phase error were less than 2 dB and 4°, respectively.

3.1 The 45° power divider

Figure 3(a) shows the circuit configuration of the proposed 45° power divider, which included a compensation capacitor (C_1) and a compensation resistor (R_2). The 45° power divider consisted of a band-pass filter and a high-pass filter using resistance-capacitance networks. Phase $\theta_b(\omega)$ of the band-pass filter, which consisted of C_1, C_3, and R_1, is given by

$$\theta_b(\omega) = \tan^{-1}\left\{-\frac{b}{a}\times\omega + \frac{c}{a\times\omega}\right\}, \quad (1)$$

$a = 1 + (Z_s + R_1) / Z_l + C_3 / C_1$,
$b = (Z_s + R_1) \times C_3$,
$c = (Z_l \times C_1)$.

Phase $\theta_{h2}(\omega)$ of the high-pass filter, which consisted of C_2, R_2, and R_3, is given by

$$\theta_{h2}(\omega) = \tan^{-1}\left\{\frac{e}{d\times\omega}\right\}, \quad (2)$$

$d = 1 + (Z_s + R_2) \times (1/Z_l + 1/R_3)$,
$e = (1/Z_l + 1/R_3) / C_2$.

Equation 1 shows that the phase characteristics of the band-pass filter had one inflection point as a function of the frequency. Equation 2 shows that the phase characteristics of the high-pass filter decreased monotonically as a function of the frequency. Therefore, because the phase difference between ports 2 and 3 in Fig. 3(a) had at most two extreme values, this divider was capable of wideband performance.

Figure 3(b) shows the S-parameter simulation results. The lumped passive elements were set so that the amplitude difference was 0 dB and the phase difference was 45° at 1.0 GHz. The phase difference had two extreme values. Hence, this divider exhibited wideband performance.

3.2 In-phase power divider

Figure 4(a) shows the circuit configuration of the in-phase power divider, which included a compensation capacitor (C_c). Under even-mode excitation, this divider is a fifth-order high-pass filter. Thus, reflection characteristic S_{11} had at most two minimum values. Reflection characteristic S_{22} and isolation characteristic S_{32} also had at most two minimum values. This is because the resonant point increased as a result of adding the compensation capacitor. This divider thus satisfied the matching conditions at two frequencies, which enabled it to also achieve wideband performance.

Figure 4(b) shows S-parameter simulation results for the in-phase power divider. The lumped passive elements were set so that the matching conditions were satisfied at 0.8 and 1.2 GHz. The divider's S_{11}, S_{22}, and S_{32} each had two minimum values and thus

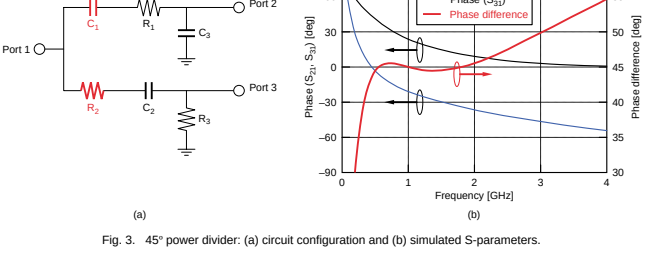


Fig. 3. 45° power divider: (a) circuit configuration and (b) simulated S-parameters.

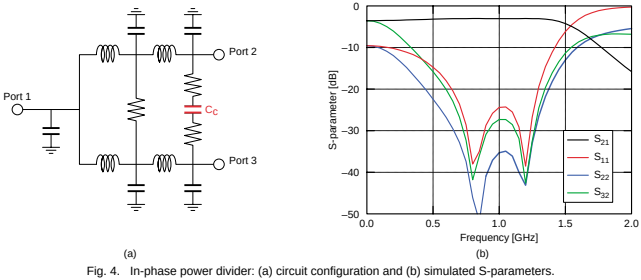


Fig. 4. In-phase power divider: (a) circuit configuration and (b) simulated S-parameters.

satisfied the matching conditions at two frequencies, which, again, enabled it to achieve wideband performance.

3.3 Fabrication and measurement results

The wideband quadrature mixer was designed and fabricated using a 0.3-μm GaAs MESFET (MEtal–Semiconductor Field Effect Transistor) process with f_t = 20 GHz and f_{max} = 70 GHz. A photograph of the chip is shown in Fig. 5. The size was 1.8 × 2.3 mm^2.

The measured amplitude balance and the quadrature phase error of the output signals for demodulation are shown in Fig. 6. The frequency of the baseband signal was set at 144 kHz (not zero), the RF power level at –20 dBm, and the LO power level at +5 dBm. When the RF signal frequency was between 0.9 and 2.5 GHz, the amplitude balance and the quadrature phase error were less than 1.6 dB and 3º, respectively.

We tested the modulation performance using the single-side-band method, in which the image ratio corresponds to the amplitude balance and the quadrature phase error [10]. Figure 7 shows the RF output power as a function of the frequency. A 144-kHz baseband signal with a phase difference of 90º was input. The frequency was converted into an RF signal of frequency f_{RF} based on the LO signal of frequency f_P = (f_{RF} – 144 kHz)/2. The input voltage of the baseband signal was 500 $mV_{p\text{-}p}$. The input level of the LO signal was +5 dBm from 0.7 to 2.3 GHz and +10 dBm at 2.4 GHz or higher. When the RF signal frequency was between 0.9 and 2.5 GHz, the image ratio was less than –30 dBc and the leakage signal level at frequency $2f_P$ was less than –40 dBm. This image ratio

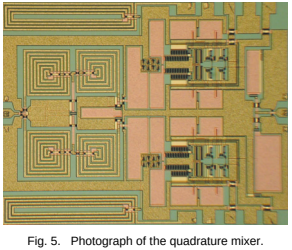


Fig. 5. Photograph of the quadrature mixer.

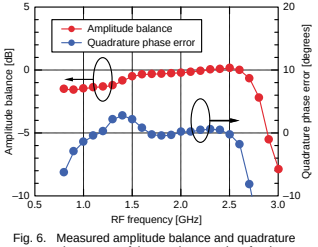
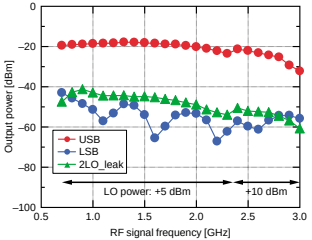


Fig. 6. Measured amplitude balance and quadrature phase error of the quadrature mixer for the demodulator.



USB: upper sideband; LSB: lower sideband

Fig. 7. Measured output signals and leakage signals of the quadrature mixer for the modulator.

indicates that the quadrature phase error was less than 3.6º if we assume an amplitude balance of 0 dB.

4. Low-noise variable-gain amplifier

The variable-gain amplifier controls the gain in the IF stage of transceivers with a superheterodyne architecture. However, there is no IF stage in transceivers with a direct conversion architecture. Consequently, a gain-control mechanism was needed in the RF stage. We therefore developed an LNVGA for that stage. The design targets for the gain, noise figure, and variable-gain control range were above 20 dB, below 4 dB, and above 30 dB, respectively.

Figure 8 shows its circuit configuration. To achieve wideband characteristics, no matching circuits with reactance elements were used. The amplifier used a variable-feedback circuit that consisted of two ASFs (Anti-Series FETs) and two capacitors. The ASF circuit remained unsaturated with input power greater than the power which would cause a single FET to saturate. As a result, the ASF circuit had lower distortion than a single FET [7]. Therefore, when the amplifier's gain was controlled, the amplifier was capable of low distortion.

The LNVGA was fabricated using 0.15-μm GaAs pHEMT (pseudomorphic High Electron Mobility Transistor) technology and had two-stage amplifiers. A photograph of the chip is shown in Fig. 9. The size was 1.3×2.0 mm^2. The measured gain response, noise figure, and IP3 (3rd Intercept Point) are shown in Figs. 10, 11, and 12, respectively. From 0.9 to 2.5 GHz, the maximum gain was more than 26 dB, the

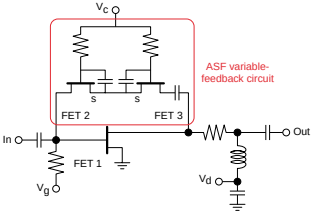


Fig. 8. Circuit configuration of the low-noise variable-gain amplifier.

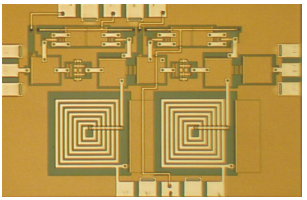


Fig. 9. Photograph of the low-noise variable-gain amplifier.

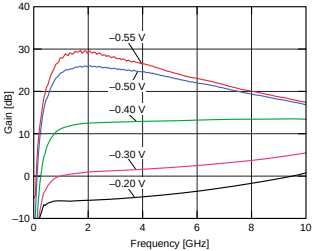


Fig. 10. Measured gain response of the low-noise variable-gain amplifier.

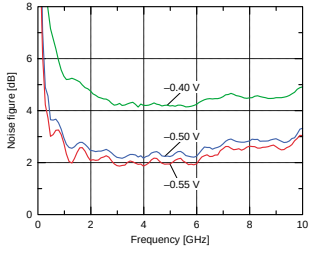
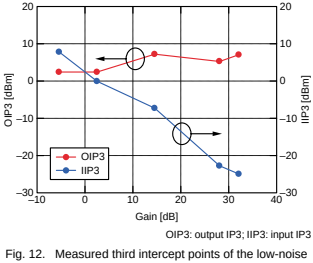


Fig. 11. Measured noise figure of the low-noise variable-gain amplifier.



OIP3: output IP3; IIP3: input IP3

Fig. 12. Measured third intercept points of the low-noise variable-gain amplifier.

noise figure at the maximum gain was less than 3.1 dB, and the variable-gain control range was more than 30 dB. Moreover, when the LNVGA gain was changed, the OIP3 (Output IP3) remained almost constant near the value before the change.

5. Local oscillator

Our goal was to build a local oscillator that would be able to cover the frequency bands of the target systems shown in Table 1. This LO would require only a few commercially available VCOs (Voltage-Controlled Oscillators), and would have a tuning bandwidth within 10% of the center frequency. The actual LO, whose architecture is shown in Fig. 13, has only two VCOs. Variable frequency dividers with four SPDT (Single Pole Double Throw) switches were also used. Phase noise was reduced by using frequency division. Thus, the phase noise requirements were not severe. This architecture was able to cover all three systems from 0.9 to 2.5 GHz, including the FDD system. In the FDD settings, the target suppression level for the leakage signal was more than 50 dB.

A block diagram of the variable frequency divider is shown in Fig. 14. Dual-modulus prescalers and selectors were used because programmable counters cannot operate at high frequencies. The frequency division ratios were 2, 3, 4, 5, and 6. The variable frequency divider included an additional half frequency divider that was used for PLL (Phase-Locked Loop) input because many commercially available ICs for PLLs operate at less than 2.5 GHz. The variable frequency divider was fabricated using a silicon bipolar process with $ft = 35$ GHz. A photograph of the chip is shown in Fig. 15. The size was 2.0×2.0 mm^2. The fabricated variable frequency divider operated in the frequency range of 100 MHz to 3.4 GHz when the

Table 1. Parameters for local oscillator settings.

Required tuning frequency range of VCO 1: 2402-2655 MHz.
Required tuning frequency range of VCO 2: 2694-2877 MHz.

System	Duplexing	Frequency band specification (MHz)	Settings selected for the frequency divider output	Division ratio of the variable frequency divider	Double the frequency of the frequency divider output (MHz)
PDC	FDD	RX 810-885	Divider 1 (to RX)	6	801-885
		TX 898-956	Divider 2 (to TX)	6	898-959
PHS	TDD	1895.15-1917.95	Divider 2 (to TX,RX)	3	1796-1918
2.4-GHz wireless LAN	TDD	2402-2484	Divider 1 (to TX,RX)	2	2402-2655

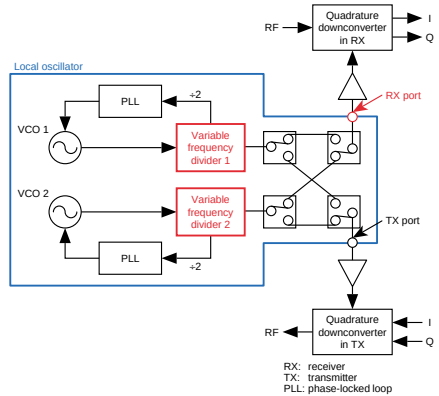


Fig. 13. Block diagram of the local oscillator architecture.

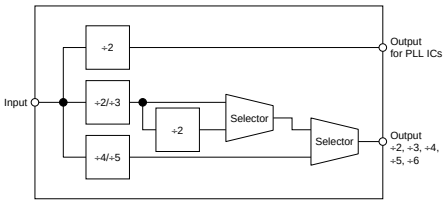


Fig. 14. Block diagram of the variable frequency divider.

input power was −10 dBm. This showed that it was possible to achieve all the frequencies in Table 1. The VCOs and the switches were commercially available products. The tuning ranges of the two VCOs were from 2.38 to 2.69 GHz and from 2.65 to 3.02 GHz with a 3-V supply. The SPDT switches had 0.6 dB of insertion loss and 40 dB of isolation from DC to 2.5 GHz.

Figure 16 shows the output spectrum of the local oscillator at the RX port shown in Fig. 13 for the FDD system settings. The leakage signal level of 478 MHz was suppressed by more than 60 dB compared with the desired signal level of 413 MHz.

6. Conclusion

We have developed an RF chipset for multi-band direct conversion transceivers that covers the frequency bands of three systems (PDC, PHS, and 2.4-GHz WLAN). The chipset consists of a quadrature mixer, an LNVGA, and a local oscillator. The mixer achieves wideband performance through the use of newly developed wideband power dividers. When the RF frequency was between 900 MHz and 2.5 GHz,

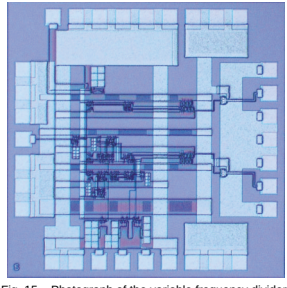
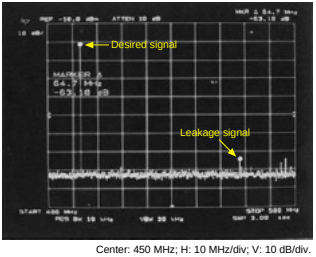


Fig. 15. Photograph of the variable frequency divider.



Center: 450 MHz; H: 10 MHz/div; V: 10 dB/div.

Fig. 16. Output spectrum of the local oscillator.

the demodulator mixer experimentally showed an amplitude error of less than 1.6 dB and a quadrature phase error of less than 3º. For the same RF frequency range, the modulator mixer showed an image ratio of less than –30 dBc. The LNVGA achieves wideband performance without the use of reactance elements and displays highly linear performance through the use of an anti-series FET feedback circuit. From 900 MHz to 2.5 GHz, the maximum gain is more than 28 ± 1.6 dB, the noise figure at the maximum gain less than 3.1 dB, and the variable-gain control range more than 30 dB. The local oscillator achieves multi-band performance that is able to cover the target frequencies for PDC, PHS, and 2.4-GHz WLAN systems.

This approach should significantly contribute to the development of compact multi-mode mobile transceivers such as software-defined radios.

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