

Monolithically Integrated 64-channel WDM Channel Selector

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Abstract

Wavelength division multiplexing (WDM) channel selectors will be key devices in future photonic networks. In this paper, we describe a novel WDM channel selector configuration that lets the selector handle a large number of WDM channels. The selector consists of two arrayed waveguide gratings, two stages of semiconductor optical amplifier gates, and a coupler. Based on this configuration, we developed the first monolithically integrated 64-channel WDM channel selector on an InP substrate. Loss-less operation was achieved for all channels. The typical sensitivity penalty for a 10-Gbit/s NRZ (non-return to zero) signal was measured to be 1.3 dB. Fast switching of less than 1.5 ns was obtained.

1. Introduction

The rapid increase in the volume of data traffic due to improvements in Internet technologies is making it necessary to enhance network throughput. Wavelength division multiplexing (WDM) systems can meet this demand, and they are being introduced commercially. WDM systems can also improve network flexibility through wavelength routing and are promising for future photonic networks. In such networks, various kinds of functional devices will be required. One of them is a WDM channel selector that can select and output an arbitrary signal from WDM signals. It will be used in an optical add-drop multiplexer (OADM) and optical cross-connect (OXC). In addition, a tunable WDM light source can be constructed by using a selector with a multi-channel laser array, and a wavelength-selective receiver can also be made by combining a selector with a photodiode.

The WDM channel selector has already been developed using two arrayed waveguide gratings (AWGs) and semiconductor optical amplifier (SOA) gates [1]–[8]. This type of selector has very attractive features, such as a high extinction ratio, loss-less operation, and nanosecond channel switching time. The largest

number of channels reported so far is 16 for monolithic integration [2] and 32 for hybrid integration [3]. However, these conventional selectors need as many optical gates as WDM channels. As the number of WDM channels increases, integration will become more difficult from the viewpoints of chip size, fabrication yield, assembly, and number of electrical drivers.

We recently proposed a novel configuration that enables the WDM channel selector to handle a larger number of WDM channels [9]. The idea is to reduce the number of optical gates in a WDM channel selector by using the cyclic function of the AWG and a two-step process for selection. In this paper, after reviewing the selector configuration and operating principle we discuss the design and fabrication processes and then report the performance of a fabricated monolithically integrated 64-channel WDM channel selector based on the new configuration.

2. Configuration and principle

Our WDM channel selector consists of two AWGs, two arrays of SOA gates, and a coupler as shown in Fig. 1. The $1 \times M$ AWG is designed to have a channel spacing of $\delta\lambda$ (equal to the grid spacing) and a free spectral range (FSR) of $M\delta\lambda$. On the other hand, the $M \times N$ AWG is designed to have a channel spacing of $M\delta\lambda$ and an FSR of $(M \times N)\delta\lambda$. Let us consider the operating principle. Due to the cyclic function of the

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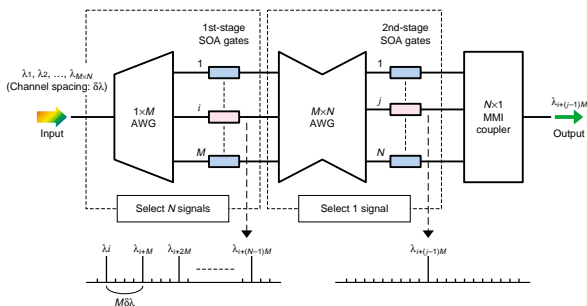


Fig. 1. Schematic diagram of proposed configuration of WDM channel selector.

AWG, the incoming ($M \times N$) signals are distributed to M output ports by N signals, which have a spacing of $M\delta\lambda$ (equal to the FSR of the $1 \times M$ AWG). Turning on the i -th gate of the 1st-stage SOA gates launches the corresponding N signals of $\lambda_{i+M}, \lambda_{i+2M}, \dots, \lambda_{i+(N-1)M}$ into the $M \times N$ AWG. The others are absorbed (1st-step selection). Next, the selected N signals are demultiplexed by the $M \times N$ AWG into its N output ports. After that, one signal of $\lambda_{i+(j-1)M}$ is selected and output through the $N \times 1$ multi-mode interference (MMI) coupler (2nd-step selection). Thus, any one of the input signals can be selected with the appropriate combination of i and j . In this configuration, the total number of SOA gates is only $(M+N)$, which is considerably fewer than the $(M \times N)$ of the conventional configuration. Figure 2 shows an example for 16 channels ($M=N=4$). Figures 2(a) and (b) show the input/output tables of the 1×4 and 4×4 AWGs. Figure 2(c) shows the relationship between the combinations of the SOA gates and the output from the 16-channel WDM channel selector.

3. 64-channel WDM channel selector

We have demonstrated a monolithically integrated 64-channel WDM channel selector with a grid spacing of 50 GHz on an InP substrate ($M=N=8$) based on the new configuration. This selector needs only 16 gates in total, whereas a conventional one needs 64 gates.

3.1 Device structure

(1) Semiconductor AWG

The channel spacing and FSR of the 1×8 AWG are 50 and 400 GHz, respectively. For the 8×8 AWG, they are 400 GHz and 3.2 THz, respectively. We used a high-mesa structure for passive waveguides because its low propagation loss and high horizontal optical confinement let us reduce the chip size. The core layer is a $0.5\text{-}\mu\text{m}$ -thick InGaAsP with a bandgap wavelength of $1.05\ \mu\text{m}$. The waveguide width is $2.5\ \mu\text{m}$.

(2) MMI coupler

The MMI coupler has several benefits, such as a compact size, a wide wavelength range, small polarization-dependent loss (PDL), and suitability for integration. For a 64-channel WDM channel selector, we used an 8×1 MMI coupler with a high-mesa structure and the same layer structure as the AWGs. Using the same structure for both the AWGs and the MMI coupler allows us to fabricate them at the same time. The MMI section is $32\ \mu\text{m}$ wide and $260\ \mu\text{m}$ long. The input- and output-waveguides are $2.5\ \mu\text{m}$ wide and their pitch at the input interface is $4.0\ \mu\text{m}$.

Figure 3 shows the fiber-to-fiber transmittance of the fabricated 8×1 MMI coupler. Sixteen transmittances from eight input ports for the transverse electric and magnetic modes (TE and TM modes) are plotted and the upper two lines are the transmittances of a reference straight waveguide for both modes. The loss of the reference straight waveguide represents the sum of the propagation loss and fiber coupling

Output	1	$\lambda_1, \lambda_5, \lambda_9, \lambda_{13}$			
	2	$\lambda_2, \lambda_6, \lambda_{10}, \lambda_{14}$			
	3	$\lambda_3, \lambda_7, \lambda_{11}, \lambda_{15}$			
	4	$\lambda_4, \lambda_8, \lambda_{12}, \lambda_{16}$			

(a)

		Output			
		1	2	3	4
Input	1	$\lambda_1, \lambda_2, \lambda_3, \lambda_4$	$\lambda_5, \lambda_6, \lambda_7, \lambda_8$	$\lambda_9, \lambda_{10}, \lambda_{11}, \lambda_{12}$	$\lambda_{13}, \lambda_{14}, \lambda_{15}, \lambda_{16}$
	2	$\lambda_5, \lambda_6, \lambda_7, \lambda_8$	$\lambda_9, \lambda_{10}, \lambda_{11}, \lambda_{12}$	$\lambda_{13}, \lambda_{14}, \lambda_{15}, \lambda_{16}$	$\lambda_1, \lambda_2, \lambda_3, \lambda_4$
	3	$\lambda_9, \lambda_{10}, \lambda_{11}, \lambda_{12}$	$\lambda_{13}, \lambda_{14}, \lambda_{15}, \lambda_{16}$	$\lambda_1, \lambda_2, \lambda_3, \lambda_4$	$\lambda_5, \lambda_6, \lambda_7, \lambda_8$
	4	$\lambda_{13}, \lambda_{14}, \lambda_{15}, \lambda_{16}$	$\lambda_1, \lambda_2, \lambda_3, \lambda_4$	$\lambda_5, \lambda_6, \lambda_7, \lambda_8$	$\lambda_9, \lambda_{10}, \lambda_{11}, \lambda_{12}$

(b)

		2nd-stage SOA gate			
		1	2	3	4
1st-stage SOA gate	1	λ_1	λ_5	λ_9	λ_{13}
	2	λ_6	λ_{10}	λ_{14}	λ_2
	3	λ_{11}	λ_{15}	λ_3	λ_7
	4	λ_{16}	λ_4	λ_8	λ_{12}

(c)

Fig. 2. Example of the AWG design for the selector (16 channels). (a) Output of the front AWG (1×4), (b) input/output of the rear AWG (4×4), and (c) selector output corresponding to the 1st- and 2nd-stage SOA gates.

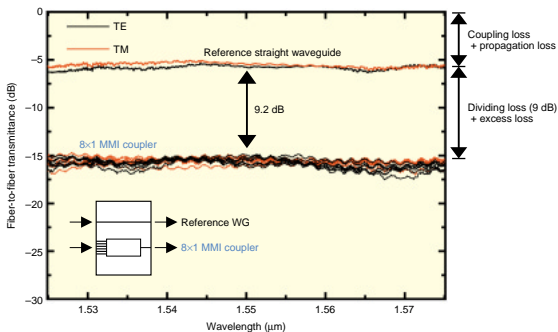


Fig. 3. Fiber-to-fiber transmittance of the 8×1 MMI coupler.

loss. The transmittance difference between the reference straight waveguide and the 8×1 MMI coupler includes the dividing loss of 9 dB and the excess loss. We confirmed uniform, flat transmittances over a wavelength range of 50 nm. This is wide enough for the 64-channel WDM channel selector with a channel spacing of 50 GHz (about 26 nm). We obtained a very small minimum excess loss of only 0.2 dB and the average inter-port PDL was 0.5 dB.

(3) SOA gates

We used a ridge waveguide structure for the SOA gates. The active layer is 0.2- μm -thick InGaAsP ($\lambda_g = 1.53 \mu\text{m}$) with a 0.1- μm -thick upper SCH (separate-confinement heterostructure) layer ($\lambda_g = 1.2 \mu\text{m}$). The ridge waveguide is 2.0 μm wide and 600 μm long. Its structure does not need embedding regrowth, which helps keep the monolithic integration simple. Below, we describe our monolithic integration for the semiconductor AWG, MMI coupler, and SOA gates.

3.2 Fabrication process

The fabrication procedure is shown in Fig. 4. The SOA's layer structure is grown first using metal organic vapor phase epitaxy (MOVPE). Next, the passive region is etched down to the interface between the active and lower cladding layer. Then, the core and upper cladding layers of the passive region are grown using MOVPE and butt-joined to the SOAs. After that, the ridge waveguides for the SOAs are formed by dry and wet etching. The SCH layer acts as an etch-stop layer in this step. Finally, the high-mesa structure for passive devices is made

using $\text{Br}_2\text{-N}_2$ RBE (reactive beam etching) [10]. As mentioned above, we use regrowth only once, which simplifies the fabrication process.

Figure 5 shows a microscope photograph of a fabricated 64-channel WDM channel selector. A booster SOA, which equalizes the output power, is also integrated into the selector and its structure is identical to that of the SOA gates. The total chip size is $7.0 \times 7.0 \text{ mm}^2$. Using this fabrication process, we successfully made a high-mesa waveguide with very low propagation loss of between 1 and 2 dB/cm.

3.3 Device performance

First, we investigated the current-gain characteristics of the integrated SOA. The SOA was 600 μm long and joined with passive waveguides on both

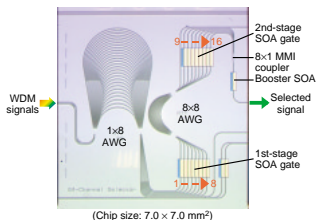


Fig. 5. Microscope photograph of the fabricated 64-channel WDM channel selector.

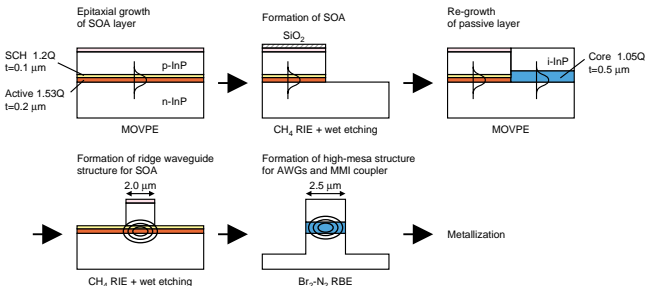


Fig. 4. Fabrication process.

sides. The total length of the passive waveguides was 8 mm. Figure 6 shows the fiber-to-fiber gain curves for the TE and TM modes. The wavelength of the input signal was 1565 nm with an optical power of -10 dBm. A fiber-to-fiber gain of more than 5 dB was achieved. This result indicates that the SOA has a net gain of about 15 dB.

Next, we investigated the static characteristics of the fabricated 64-channel WDM channel selector. Figure 7(a) shows a photograph of the selector module, and Fig. 7(b) shows its superimposed fiber-to-fiber transmittance when the input optical power was 0 dBm. The wavelength range we used was 1547.72 to 1573.30 nm (190.55 to 193.7 THz). We successfully confirmed selection and obtained loss-less operation for all 64 channels. The background level was under -25 dB.

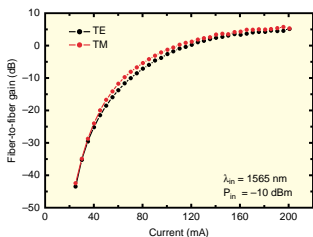
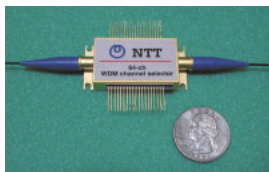


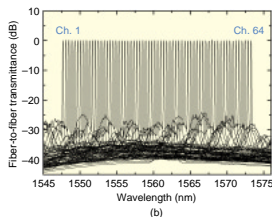
Fig. 6. Fiber-to-fiber gain of ridge-waveguide structure SOA.



(a)

We also investigated the bit-error-rate (BER) characteristics of the fabricated selector. The input signal was modulated by a 10-Gbit/s NRZ (non-return to zero) signal with PRBS (pseudorandom bit sequence) of $2^{31}-1$ and its average power was $+2.5$ dBm. Error-free operation for all channels was confirmed. As an example, Fig. 8 shows the eye diagrams of the signal entering and exiting the selector for ch. 64 ($\lambda_{64} = 1573.30$ nm, the longest wavelength channel) and the BERs of Ch. 1 ($\lambda_1 = 1547.72$ nm, the shortest wavelength one) and Ch. 64. Clear eye openings were observed. The sensitivity penalties of the two channels were 1.8 (Ch. 1) and 1.0 dB (Ch. 64). These penalties are mainly attributable to an upward shift of the space-level due to the amplified spontaneous emission noise of the booster SOA. The sensitivity penalties of other channels were also measured. Figure 9 shows the histogram of the sensitivity penalties for all channels at a BER= 10^{-9} . Small sensitivity penalties with a typical value of 1.3 dB were obtained. The minimum was 0.4 dB and the maximum 2.1 dB.

Finally, we show the channel switching characteristics of the fabricated selector. For ease of explanation, we number the gates 1 to 16, as shown in Fig. 5. In this experiment, the 2nd-stage SOA gate, which was turned on, was fixed and it was gate 13 throughout. Gates 3 and 5 as the 1st-stage SOA gate were turned on alternately every 32 ns. Channel 14 was selected when gates 3 and 13 were turned on, and ch. 60 when gates 5 and 13 were turned on. Figure 10 shows the switching characteristics. 10-Gbit/s and 2.5-Gbit/s NRZ signals were used for channels 14 and 60, respectively. We obtained fast switching: the rise-time was less than 1.5 ns and the fall-time less than 1.0 ns.



(b)

Fig. 7. Static characteristics of fabricated 64-channel selector module.

(a) Photograph of module and (b) fiber-to-fiber transmittance.

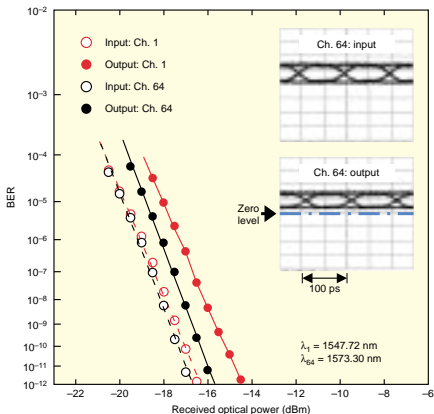


Fig. 8. Bit error rate characteristics.

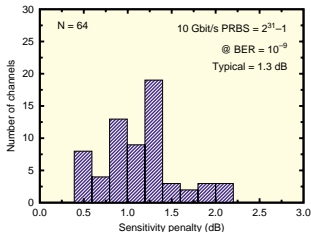


Fig. 9. Histogram of sensitivity penalties for all 64 channels.

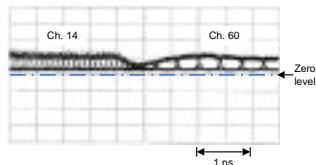


Fig. 10. Channel switching characteristics.

4. Summary

Our novel WDM channel selector configuration enables the selector to handle a large number of WDM channels. Based on this configuration, we demonstrated the first monolithically integrated 64-

channel WDM channel selector. Channel selection and loss-less operation for all channels were successfully achieved. We also measured the BERs at 10 Gbit/s and confirmed error-free operation for all channels. The typical sensitivity penalty was 1.3 dB. We also obtained fast channel switching of less than 1.5 ns.

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