Recent Progress in Optical Packet Processing Technologies for Optical Packet-switched Networks

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Abstract

Among photonic multiprotocol label switching technologies, optical packet switching is the most attractive from the viewpoints of flexibility, scalability, and bandwidth utilization efficiency. However, the technical barriers to achieving the functions required in the networks, such as optical label processing and contention resolution, are still very high. In this paper, I discuss the various benefits of and difficulties in optical packet-switching technology and outline recent progress in optical packet processing technologies towards overcoming those difficulties. I also describe the concepts and advantages of our systems based on hybrid optical/electrical technology, which makes optimum use of all-optical, optoelectronic, and electronic devices.

1. Introduction

The growth of the Internet and Internet-related services has caused Internet protocol (IP) data traffic to overtake voice traffic faster than predicted by the well-known Moore's law. To cope with this explosive growth of IP traffic, we must not only increase link capacity by using wavelength division multiplexing (WDM) technology, but also improve the throughput of nodes by introducing specific optical technologies. In addition, the entire network must be optimized at all levels (especially the backbone and metropolitan levels) for IP data traffic and the underlying IP support protocols. The optimization must take into consideration three fundamental requirements: flexibility of resource allocation and reallocation (traffic engineering, protection, rerouting, various services, etc.), scalability of network topologies and algorithms, and cost effectiveness.

Current data networks are typically constructed with four stacked layers: an IP layer for carrying applications and services, an asynchronous transfer mode (ATM) layer for traffic engineering, a synchronous optical network/synchronous digital hierarchy (SONET/SDH) layer for transport, and a dense WDM layer for capacity. Although this separation into layers provides some benefits, it also leads to inefficiencies, increases the latencies of connections, and inhibits the provisioning of quality of service (QoS) assurances. Furthermore, the layers are largely unaware of each other, so there is some duplication of transport protocols and management tasks [1]. Therefore, optimizing the network to achieve flexibility, scalability, and cost effectiveness will require a simplified layer configuration.

Multiprotocol label switching (MPLS) technology has emerged as a promising solution. MPLS meets the above requirements because it enables us to eliminate the ATM and SONET/SDH layers and integrate an IP layer with a photonic layer. When designing the node architecture in MPLS networks, we must consider the need for high throughput, low packet loss probability, short delay, high signal quality of outgoing packets, transparency to data rate and format, small power consumption, and compactness. However, current IP routers, which rely on electronic processing, seem unable to keep up with the rapid growth of the Internet. Therefore, optical processing technologies are expected to play an important role in the switching nodes in order to meet these requirements. Three main approaches used in photonic MPLS networks are generalized MPLS (GMPLS) [2], [3], optical burst switching (OBS) [4], [5], and optical packet switching (OPS) [5]-[9].

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This paper outlines optical packet processing technologies, focusing on OPS networks and describes the concept of our approach to packet processing. The four other selected papers in this issue describe individual devices and subsystems.

2. Optical packet switching

2.1 Network evolution scenario

Photonic networks seem to have evolved in the order of GMPLS, OBS, and OPS from the viewpoint of the maturity of optical switching technologies. GMPLS utilizes wavelengths as labels and operates based on circuit-switching technology that uses optical cross-connects (OXCs) to support light paths. That is, packet-forwarding decisions are made only at edge nodes; forwarding tasks at core nodes are eliminated. This means that only switching tasks are carried out at the core nodes, which alleviates the burden on them significantly. However, GMPLS suffers from several limitations because its data granularity is too large in terms of wavelength capacity (very long switching periods). There are too few wavelengths to accommodate all the light paths required, implying poor scalability and flexibility (e.g., hundreds of clients requires thousands of connections). Furthermore, the scarcity of wavelength resources makes it difficult to support applications and services (traffic engineering, fast rerouting, virtual private networks, QoS, and so on). In addition, a very large-scale OXC switching fabric, such as one based on three-dimensional micro-electromechanical systems (MEMS) switches, is necessary in order to achieve full connectivity, but such large-scale OXC technology is still immature. Throughput is also limited because end-to-end traffic must rely on only one wavelength channel.

The data granularity of OBS lies between that of GMPLS and OPS (microsecond order). Therefore, the problems related to the granularity issue in GMPLS are alleviated to some degree. OBS has emerged as a synthesis of optical and electronic technologies. At the edge of the network, for example, packets with the same destination are assembled to form a burst, which is assigned to a wavelength channel. Before the burst is launched, an out-of-band optical control packet sets up an optical path for a fixed time period. Then, the burst is transparently switched at core nodes without any optical-to-electrical or electrical-to-optical (OE/EO) conversion.

OPS can overcome the above-mentioned granularity issue because it provides arbitrary granularity at the packet level. Since it can achieve very good time-domain statistical multiplexing performance due to its fine granularity, it has the potential to allow maximum fiber capacity utilization when it is combined with WDM technology. However, severe burdens related to label processing and contention resolution are imposed on every node. The issues concerning OPS networks are described in section 3.

2.2 Packet forwarding mechanism

In standard IP networks, all forwarding decisions are based on the destination-oriented routing protocol using destination information contained in the IP packet header, which imposes limitations on routing functionality and traffic engineering. On the other hand, for this purpose, an OPS network utilizes labels that are carried in the packet's header. These labels have fixed-length values and specify only the next hop. Packets are forwarded from one label-switching router (LSR) to another, forming label-switched paths (LSPs). The label is used to identify a forwarding equivalence class (FEC), i.e., a set of packets that are forwarded over the same path through the network. FECs are mapped to LSPs. Packets are assigned to FECs, depending on their source and destination, QoS requirements, and other parameters, and those belonging to the same FEC do not necessarily have the same destination. This is particularly advantageous because the network becomes so flexible that various applications and new services can be added by simply modifying how packets are assigned to FECs. The introduction of FECs can also reduce the number of address entries in a forwarding table to several hundred, which is minute compared with the more than 500,000 entries required in the standard IP network.

In OPS networks (as in MPLS networks), the control and forwarding components are completely separated. As a result, each component can be developed and modified independently. The control component uses the standard IP routing protocol to exchange information with other LSRs and thereby build and maintain a forwarding table. The forwarding component is based on a label-swapping forwarding algorithm (**Fig. 1**). Packets are classified and assigned their initial labels at the ingress LSR. When a labeled packet arrives at a core LSR, the label is checked against the entries in the forwarding table using an exact-match algorithm, and the output label and the outgoing interface are retrieved. The forwarding component then updates the incoming label and directs the packet to the outgoing interface across the system's switching fabric [9]. At the egress LSR, the

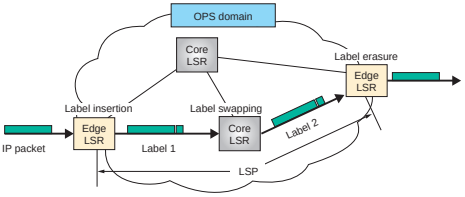

Fig. 1. Optical packet-switched network.

label is discarded and the packet is forwarded to the standard IP network using the conventional longest-match IP routing algorithm.

2.3 Synchronous and asynchronous networks

OPS networks use a synchronous (slotted) or asynchronous (unslotted) network strategy [8]. In a synchronous network, all packets have a fixed length and are placed in a fixed time slot that is longer than the packet duration to allow for a guard time. The fixed-length packets imply the need to segment IP datagrams at the ingress LSRs and reassemble them at the egress LSRs. In addition, this approach imposes an additional burden for aligning the packets before they enter the space switch [10] because packet arrival times at the switch vary due to different propagation distances, chromatic dispersion in optical fibers, and environment temperature changes. Maintaining input synchronization would be a severe task in the optical domain. It is possible to statically compensate for such delay variations using fiber delay lines (FDLs), but dynamic compensation in a packet-by-packet manner would be difficult. However, the input synchronization makes it easy to utilize optical FDL buffers for packet contention resolution as described in section 3.2.

On the other hand, asynchronous networks can handle packets with variable lengths and do not require packet segmentation and reassembly at the edge LSRs, which makes the network more suitable for native IP packets. Furthermore, a simpler node architecture is possible because no burdensome synchronization mechanism is needed. However, the unpredictable behavior of asynchronous packets increases the probability of packet contention, which reduces network throughput and increases the packet loss ratio. In addition, contention resolution using FDL buffers often produces a long gap or void between the output packets due to the fixed large granularity of the optical FDL buffer, resulting in further reduction of the network throughput. Therefore, a complex scheduling algorithm must be implemented to schedule new arrivals asynchronously [11].

3. Optical packet processing technologies

Resolving the issues in OPS networks will require many technical breakthroughs in several areas:

- optical label processing (recognition/swapping)
- optical packet contention resolution
- clock extraction (bit/packet-level synchronization)
- optical packet compression/decompression
- optical space switching
- wavelength conversion
- 3R (reamplification, reshaping, retiming) regeneration

This section concentrates on optical label processing and optical packet contention resolution.

3.1 Optical label processing

In electrical networks, the packet header is transmitted serially with the payload at the same data rate. However, as the data rate increases in optical networks, implementing an electrical header processor operating at such high speed to switch packets on the fly at every node becomes more difficult.

Among several different proposed solutions, the subcarrier multiplexed (SCM) label transmission scheme [12], [13] is attractive for packets at 10 Gbit/s or less. In the SCM scheme, label bits are encoded on the data payload using a properly chosen subcarrier frequency at a lower bit rate (**Fig. 2(a)**). This approach enables the label recognition and swapping procedures to be performed either electrically or optically. However, the subcarrier frequency must usually be higher than the payload data rate so that it does

not overlap with the baseband. This means that expensive high-speed microwave components (e.g., local oscillators, modulators, mixers, receivers, and filters) are required, and the payload data rate is limited to rates that are much lower than the operating speed of the microwave electronic devices. Recently, a technique based on dispersion-division multiplexing has been demonstrated to overcome this limitation [12].

A method of transmitting a label that has a different wavelength from the payload has been proposed (**Fig. 2(b)**) [14], [15]. In this approach, low-bit-rate labels are usually used, and the label processing becomes independent of the payload data rate. This approach also simplifies the procedure of packet insertion and erasure at edge LSRs by using passive wavelength multiplexing/demultiplexing. Furthermore, the label can be easily recognized and updated using conventional electronic devices. However, this approach suffers from the chromatic dispersion of the optical fiber; hence, the timing of label and payload arrivals often fluctuates due to changes in the ambient temperature. In addition, it wastes the wavelength resources in WDM systems because each wavelength channel requires a different wavelength for the label.

Another approach is to transmit a label and payload serially on the same wavelength. Guard times are

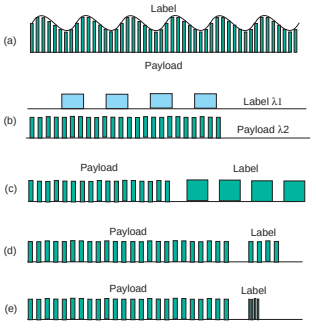

Fig. 2. Label transmission schemes. (a) Subcarrier-multiplexed label, (b) wavelength label, (c) slow serial-bit label, (d) baseband label, and (e) OCDM label.

necessary before and after the payload to prevent damage during label erasure or insertion. In this approach, low-bit-rate labels (**Fig. 2(c)**), baseband labels **(d)**, or optical code-division multiplexed (OCDM) labels **(e)** can be used. Like the methods described above, the low-bit-rate labels can be easily processed without burdening electronic circuits. However, if the label bit rate is too low, the occupation ratio of the label in the entire packet, especially in a high-speed short packet, increases, resulting in reduced throughput in the network. In addition, it takes longer to retrieve label information, which results in longer payload delays.

The OCDM labels are transmitted as high bit-rate BPSK (binary phase shift keying) optical codes encoded by a PLC (planar lightwave circuit)-based optical transversal filter that monolithically integrates tunable taps, delay lines, optical phase shifters, and a combiner [16]. The OCDM label is decoded using the transversal filter at the receiver side. When the filter is the counterpart of the transmitter's transversal filter, the output auto-correlation waveform shows a sharp peak at the center. Otherwise, there is no peak in the cross-correlation waveform. Therefore, by thresholding the correlation output, the input label can be identified. A 200-Gchip/s 128-chip hierarchical OCDM label transmission has been successfully demonstrated. This technique can carry out label recognition in an all-optical fashion simply using passive optical devices. As a result, the processing speed is very fast because it is determined by the speed of light in the device. The OCDM label swapping technique has also been demonstrated using an XPM-induced phase shift in a long optical fiber (XPM: cross phase modulation) [17].

A baseband label is transmitted with an NRZ (non-return to zero) or RZ pattern at the same bit rate as the payload on the same wavelength. Several all-optical pattern-matching techniques have been proposed for baseband label processing to alleviate the burden on the electronics and shorten the processing time. These include a passive optical correlator composed of an array of fiber Bragg gratings as tunable reflectivity mirrors [12], an all-optical comparator that uses a spin-polarized semiconductor optical switch [18], and an all-optical AND gate based on a semiconductor optical amplifier [19]. However, in mesh networks (unlike ring networks), these methods as well as the OCDM method require as many devices as the number of entries (of the order of hundreds) in a forwarding table. Alternative solutions have been proposed using active time-to-wavelength [20], [21] or time-to-

space mapping [22], [23] techniques. Since these methods convert an input high-speed serial label into parallel bits, label recognition can be performed using electronics on a bit-level basis. However, almost all of these methods require as many ultrafast all-optical switches as label bits. Several new approaches have begun using unique techniques, such as optical digital-to-analog conversion [24], time-to-space conversion [25], and angular multiplexed spectral holograms [26], to enable the checking of two or more entries by one device.

3.2 Contention resolution

Contention is an inevitable problem that arises when we try to make maximum use of the bandwidth of a single WDM channel in packet-switched networks. Any solution adopted to resolve the contention strongly affects the overall network performance. Contention resolution methods are divided into three categories: buffering, deflection routing, and wavelength conversion [8].

Buffering, which exploits the time domain, is fundamental to contention resolution. It is widely used in today's electronic routers, where contention is usually resolved by a store-and-forward technique made possible by the availability of silicon random access memory (RAM), which is a mature technology that provides many advantages, including large capacity, long-term storage, random access at an arbitrary timing, low cost, compactness, reliability, controllability, and low power consumption. However, since silicon RAM is very slow (less than 1 GHz), we require expensive high-speed electronic devices to handle the high-speed optical packets, such as photodetectors (OE conversion), GaAs-based electronic demultiplexers/multiplexers, and electroabsorption modulators (EO conversion), at the input and output interfaces of the silicon RAM. The all-electronic approach may make it difficult to handle burst-mode optical packets unless a long series of preamble bits is attached to the packet in asynchronous networks or dummy packets are inserted into blank slots in synchronous networks. In addition, such an approach may limit the packet bit rate to about 10 Gbit/s because of limitations on the operating speed of the electronic components, their susceptibility to electromagnetic interference, and their large power consumption.

Unfortunately, all-optical RAM does not currently exist. Therefore, the only viable technique available for buffering in the optical domain is to use FDLs [27]-[29]. Contending packets are sent along an additional fiber length and thus delayed for a specific amount of time. The operation is based on strict first-in first-out (FIFO) queues with fixed delays. FDL buffers can be further categorized into two types: feedback and feed-forward. A feedback buffer is basically composed of a circulating loop fiber, a 2×2 switch, and an optical amplifier that compensates for the round-trip loss (**Fig. 3(a)**). A feed-forward buffer consists of either multistage 2×2 switch elements with FDLs (**Fig. 3(b)**) or a splitter, FDLs, optical gate switches, and a combiner (broadcast-and-select type) (**Fig. 3(c)**). It can provide a fixed number of optical paths of various discrete lengths. Therefore, both types restrict the packet to either a fixed length or a multiple of it. Moreover, FDL buffers have almost none of the inherent features of silicon RAM. Namely, they are bulky and expensive and do not provide large-capacity, long-term storage and random access capability at an arbitrary timing. They also suffer from a large insertion loss through their many optical components and the accumulation of amplifier noise in the fiber loops. This reduces the multi-hop capability (typically 10–20 hops in backbones) because optical signal quality is degraded by this noise. FDL buffers also require complicated control hardware and algorithms.

Deflection routing is a technique that resolves contention by exploiting the space domain [30]. If two or more packets are destined for the same output port at the same time, only one packet is allowed to proceed

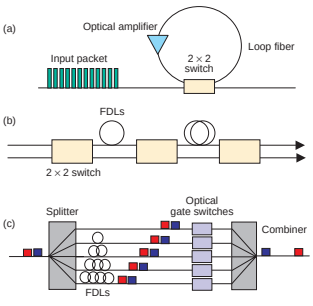

Fig. 3. Fiber delay line buffers. (a) Recirculating loop buffer, (b) multi-stage switched delay line buffer, and (c) broadcast-and-select type buffer.

to the desired output port, while the others are forwarded on different paths. The deflected packets suffer from longer delays than in the buffer solution. In addition, this approach may disturb the sequence of packets, could cause routing loops, (which increase delays and degrade signal quality for the looping packets), and increases the load on the entire network. Therefore, deflection routing without buffers (often referred to as hot-potato routing) usually results in severe performance penalties in throughput, latency, latency distribution, and packet loss probability, although it is very attractive in that there is no need to implement FDL buffers and complicated control hardware and algorithms. To keep these penalties sufficiently low, it would be helpful to employ clever algorithms, such as the second shortest path algorithm, and deflection algorithms that specifically avoid looping.

The wavelength domain, which is released from use for wavelength labels in G-MPLS networks, can be utilized for contention resolution [31]. All contending packets with the same wavelength except for one are converted to unutilized wavelengths using tunable optical wavelength converters (TOWCs). By spreading the traffic load over several wavelength channels and operating the network in a synchronous manner, the need for optical buffering is minimized or even completely eliminated. This approach can also be incorporated in an asynchronous network. However, this requires more TOWCs because one TOWC is needed for each wavelength channel at a switch input.

Each of the above methods has its advantages and disadvantages. Therefore, some combination of these techniques may provide a contention resolution strategy that offers low implementation cost, low packet delay, low packet loss probability, and high network throughput along with easy controllability, network flexibility, and high traffic engineering capability.

4. Optoelectronic approach to ultrafast asynchronous optical packet processing

As long as we ignore both cost effectiveness and the difficulty in implementing the forwarding component by optical means, OPS is obviously the best technology among the various types of photonic MPLS because it has very high-level flexibility and scalability due to its fine data granularity and can utilize the maximum bandwidth of a single channel. Furthermore, an asynchronous OPS that can handle packets of various lengths seems preferable because it is suitable for IP packets and does not need an input synchronization mechanism. Among the various label transmission schemes, the best seems to be baseband serial labels without preambles, considering the expandability of the payload data rate, low occupation ratio of the label field, and small influence of chromatic dispersion. As for the contention resolution scheme, buffering using RAM is undoubtedly ideal from the viewpoint of flexibility to applications and services, high throughput, and low packet loss rates. However, these ideal choices present tremendous technical challenges and may fail to be cost effective if things go wrong. Nevertheless, it certainly seems worthwhile trying to overcome the technical barriers by making the optimal use of optics and electronics wherever they fit best. In this section, I describe our approach to achieving the ultrafast optical packet processing required in asynchronous OPS networks.

4.1 Asynchronous baseband label processing

As discussed in section 3.1, a label recognition module must meet many requirements; e.g., it must be compact, have low latency, and be able to check an input label against all entries in a forwarding table. Furthermore, even in OPS networks, each node would need to retrieve information assigned to different fields in the header, such as TTL (time-to-live), in addition to the label information [32], [33]. If packets are misdirected or mislabeled, they never reach their destination (routing loop problem), resulting in severe network congestion. This problem is significant when deflection routing is chosen for contention resolution. To prevent this problem, the TTL value is decremented by 1 at every hop, and any packet with a TTL value of zero is dropped from the network. To retrieve different fields by all-optical pattern-matching methods, the recognition module will require a tremendously large number of pattern-matchers, which will make it huge and expensive. Meanwhile, the often-mentioned drawback of the conventional electronic system is its large power consumption. However, it is GaAs-based high-speed electronic devices, such as multiplexers/demultiplexers and amplifiers, that consume most of the power. In contrast, the silicon CMOS devices consume very little power. In addition, the silicon industry is very mature and can provide large-scale processors and memories having high functionality at very low cost. The only drawback of CMOS is its limited operating speed. Therefore, if we can make interface devices between asynchronous high-speed packets and CMOS circuits, we will achieve a breakthrough in highly func-

tional processing of ultrafast optical packets. That is our basic concept.

Figure 4 shows our approach to header/label recognition and swapping for ultrafast (40 Gbit/s or more) asynchronous optical packets [34]. This module is mainly composed of electrical/optical clock-pulse generators (ECG/OCG) [35], an all-optical serial-to-parallel converter (SPC) [23], a photonic parallel-to-serial converter (PSC) [36], and a CMOS circuit. The input header is separated from the payload by the ECG and a 1×2 optical switch, and fed into the OCG. The OCG generates a single short optical pulse accurately synchronized with the input header. Using the optical pulse as a pump pulse, the SPC performs serial-to-parallel conversion of the header. The parallel-converted optical pulses are then converted into slow electrical pulses using a low-speed photodetector (PD) array. They are launched into a CMOS processor, and then each field is retrieved. Within the CMOS circuit, for example, the TTL field is decremented by 1, and the output label and output port are decided. The updated header is output from the processor in the form of parallel electrical data when triggered by the pulse from the OCG, and reconstructed into a high-speed serial optical header by the PSC using the optical pulse from the OCG. Finally, by simply coupling the new header and the separated payload that passed through a fixed delay line, the header-swapped packet can be formed.

The SPC utilizes only one or two ultrafast surface-reflection all-optical switches (called LOTOS [37]) made with low-temperature-grown Be-doped strained InGaAs/InAlAs multiple quantum wells (MQWs). It thus has various advantages: parallel-conversion for ultrafast packets of up to 1 Tbit/s [38], scalability of the degree of parallelism, polarization insensitivity, low pump power, and compactness. Furthermore, since a LOTOS provides an extremely high extinction ratio of more than 30 dB due to a spin-polarization scheme, the SPC has high tolerance to input packet intensity fluctuations. This is a very important feature because the packet intensity often changes according to the traffic load. The current SPC module was fabricated for 16-channel parallel conversion of 40-Gbit/s packets. It is described in detail in the next paper.

To handle asynchronous optical packets, a packet-level synchronization technique is required; that is, a single clock pulse (a pump pulse for the SPC) must be created from an input asynchronous burst-mode optical packet with accurate timing. Several approaches to packet-level synchronization [39], [40] have been demonstrated in the optical domain using a semiconductor optical amplifier or an optical loop mirror. Since these schemes can extract only the first bit pulse from an input packet, the synchronization between the output optical pulse and the input packet is perfectly achieved. However, they require preamble bits with a special format or long preamble bits in front of an optical packet. In addition, they are polarization sensitive, and the intensity and polarization of the output pulse vary according to those of the input packet. Therefore, it is impossible to utilize these schemes for our SPC system because it requires a pump pulse with a fixed polarization regardless of the input packet polarization. Furthermore, conventional clock extraction based on the phase-locked loop (PLL) method cannot be used because it requires a long preamble (nanosecond order) and provides bit-level synchronization (a subsequence of "1"s). To overcome these problems, we chose to use a photoconductive sample-and-hold circuit technique for the packet-level synchronization. As a result, there is no need for extra preamble bits for clock extraction.

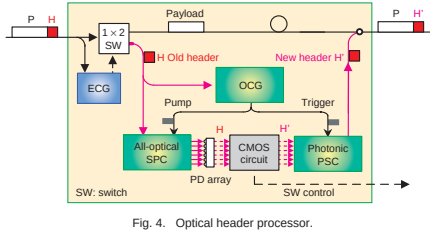

Fig. 4. Optical header processor.

Moreover, the OEO configuration enables polarization insensitivity and a wide wavelength-band. In addition, the OCG provides fixed output polarization, constant power, the desired wavelength, and accurate synchronization in spite of 10-dB input power fluctuations. Details are given in the third paper.

The PSC is also an optical/electronic hybrid system that uses photoconductive MSM-PDs (metal-semiconductor-metal photodetectors). The MSM-PD has been enhanced by adding a simple circuit and can generate 3-ps electrical pulses (the response time of an ordinary MSM-PD is more than 100 ps) [41]. Therefore, the entire PSC has the potential to generate packets at more than 100 Gbit/s. The PSC is described in the fourth paper.

Another often-cited drawback of electronic systems is the long time it takes to find an entry matching an input label. In the standard IP router, the header processing time is indeed fairly long because the entry bank is huge. However, in the LSRs, since the number of entries is small (a few hundred), the input label simultaneously checks against all entries in parallel in one try using an AND gate array in the CMOS circuit. Even a CMOS processor made with a commercial FPGA (field programmable gate array) can handle about one thousand entries. Although this procedure incurs a delay time of several tens of nanoseconds, this is negligible, compared with the delay time between nodes (a 10-ns delay corresponds to a 2-m length of fiber), and it does not limit the repetition rate of the input packets. It is the internal clock rate of the FPGA that limits the packet repetition rate (not the data rate), and a typical value is about a few hundred megahertz. Therefore, this approach can easily handle even 160-Gbit/s short packets.

4.2 Photonic RAM

As discussed in section 3.2, FDL buffers are bulky and require very complex control hardware and algorithms. Moreover, it is very difficult to use the FDL buffers in an asynchronous network. Meanwhile, we cannot expect an all-optical RAM anytime soon. Therefore, if we want a buffering technique for contention resolution in an asynchronous OPS network, it will be essential to develop a "photonic* RAM" that can read and write ultrafast asynchronous optical packets freely. Here, we use the term "photonic RAM" for a RAM that handles input and output packets in the optical domain whether stored data is electrical or optical.

Figure 5 shows the concept of our photonic RAM [42]. Its configuration is similar to the optical header processor described above. The differences are that the CMOS processor is replaced by a CMOS RAM and that the entire packet (rather than just the header) must be processed. To achieve that, the optical pulse generated from the OCG is converted using a pulse train generator (PTG) into a low-repetition optical pulse train with a period of n times the bit interval of the input packet as long as the packet continues. Then, the all-optical SPC carries out the n-parallel conversion of the optical packet in every n-bit interval successively. This data is stored in the silicon CMOS RAM. A stored packet is retrieved by specifying the address, and trigger signals with a period of n times the bit interval of the output packet (created by the PTG using a single optical pulse generated from an optical pulse source) are input in order to output n-parallel slow electrical signals simultaneously from the memory. These signals are then reconstruct-

* We use the term "photonic" to mean a device having both optical and electrical components and "optical" to mean one having only optical components and no electrical ones.

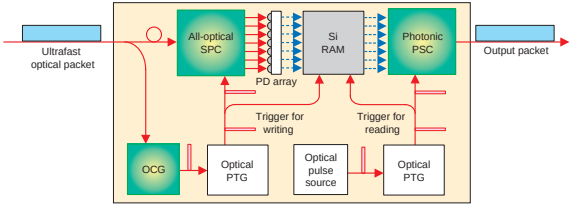

Fig. 5. Conceptual diagram of the photonic RAM.

ed into a high-speed optical packet by the photonic PSC using the optical pulse train. Thus, we can freely read and write ultrafast asynchronous optical packets of arbitrary length by specifying addresses. We have demonstrated a photonic RAM that can handle 40-Gbit/s 16-bit optical packets.

The photonic RAM has various advantages over FDL buffers (compactness, random access capability at an arbitrary timing, long-term storage, large capacity, and easy control) and over an all-electrical system that uses GaAs-based high-speed demultiplexers and multiplexers (high-speed operation at over 40 Gbit/s, low power consumption, asynchronous operation, and compactness). Furthermore, whereas the FDLs provide only buffering, the photonic RAM can provide header processing, wavelength conversion, 3R regeneration, and packet compression/decompression in addition to buffering. Details are described in the fifth paper.

Such a photonic RAM will be utilized differently at edge and core LSRs. Edge LSRs must retrieve a network layer header and assign labels to the packets. Since this procedure may take a long and unpredictable time, it is more difficult to construct the edge LSRs by all-optical means. Therefore, photonic RAMs seem more essential for the edge LSRs (**Fig. 6(a)**). Here, the RAM can act as a space switch. Meanwhile, at the core LSRs, it would be preferable to switch the payload transparently without any OEO conversion to minimize both latency and the number of components. **Figure 6(b)** shows an example for the core node architecture. Here, the contending packet, packet B, is switched to the desired port without converting the payload to an electronic signal, while packet A is sent to the photonic RAM across an optical space switch fabric and launched into the switch again at the proper timing. Such a shared buffer architecture significantly reduces the packet loss rate. In addition, since the PSC can include wavelength conversion capability, it is possible to combine it with another contention resolution method based on wavelength conversion.

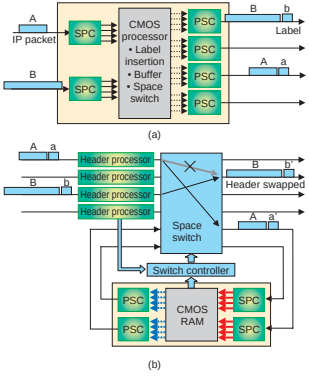

Fig. 6. Packet switch architecture for (a) edge LSR and (b) core LSR.

4.3 Other applications

A packet compression/decompression (PCD) technique is very effective for reducing the packet contention probability and enhancing network throughput [43]. Furthermore, not all networks connected to the OPS domain are operated at the same data rate and in the same format. Of course, maintaining data rate/format transparency is desirable, but it cannot be achieved as long as even one electronic component is used. Considering the difficulty in constructing edge LSRs by all-optical means at present, the packet data rate/format should be assigned to wavelengths or be unity at as high a rate as possible. Also, the packets should be transferred to a connected metropolitan or client network at the data rate/format desired by the network. Therefore, the PCD function should be installed in the edge LSRs. So far, several demonstrations of PCD have been performed in the optical domain using a fiber delay line lattice [44] or a fiber delay loop [45]. However, these systems are very complex and restricted to very short packets. In contrast, our PSC can perform PCD easily. Details of PCD are described in the fifth paper.

Our approaches described thus far assume a mesh-type network. **Figure 7** shows our concept for a ring OPS network [46]. The concept is based on a time-domain add/drop multiplexer (ADM) that has functions, such as label recognition, buffering, and PCD (e.g., between 10 and 40 Gbit/s). Here, in order to simplify switch control, a FIFO buffer rather than a RAM is used in a CMOS circuit. A packet from an input port is first stored in an input buffer and then the packet's label is checked against a local address assigned to the node. If the label matches the local address, the packet is sent to output buffer 2 for a drop

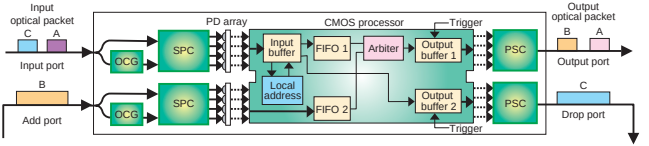

Fig. 7. Photonic time-domain add-drop multiplexer.

port. Otherwise, it is sent to FIFO buffer 1. On the other hand, a packet from an add port is sent to FIFO 2. Then, an arbiter checks FIFO 1 and 2 in order and sends the packet to output buffer 1 for an output port. Thus, add/drop multiplexing can be achieved while resolving packet contention.

5. Conclusion

Asynchronous optical packet-switched networks are the most attractive networks, at least from the viewpoint of flexibility, scalability, and bandwidth utilization efficiency. However, the technical barriers to implementing them are still very high. In this paper, I discussed the various difficult problems we face with optical packet-switched networks and outlined recent progress in optical packet processing technologies, including the concept and advantages of our systems. Since today's all-optical packet processing technologies are still immature in some aspects, there is concern, at least for the present, that the switching nodes will become very complex, huge, and expensive if all the functions required in the nodes (label recognition/swapping, buffering, 3R regeneration, PCD, switching, etc.) are achieved separately by all-optical means. In our systems, silicon CMOS processors play a very important role, just like they do in existing electronic IP routers, and this allows various functions to be integrated compactly. Almost all network researchers, especially those who work in the optics field, want to build networks in which optical technology plays the major role. I am one of them, but my current view is that the problems can be overcome only through technical breakthroughs in which we make optimal use of both optics and electronics wherever they fit best. However, recently, various novel optical devices (e.g., photonic crystal fibers/devices) and hybrid or monolithic integration technologies (e.g., semiconductors on planar lightwave circuits) have been progressing steadily. By combining these optical technologies with a clever node architecture, we should in the future be able to make transparent nodes (at least core nodes), where optical packets do not undergo OEO conversion.

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