Selected Papers

Ultrafast Optical Packet Processing Technologies Based on Novel Hybrid Optoelectronic Devices

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Abstract

We present three ultrafast optical packet processing technologies required for future optical packet-switched networks: an optical label swapper, a photonic RAM (random access memory), and a packet compressor/decompressor. These hybrid optoelectronic devices are key components of our serial/parallel-conversion-based optoelectronic system that can process ultrafast asynchronous burst optical packets functionally using slow but smart CMOS circuits with low power consumption.

1. Introduction

Optical packet switching needs many functions including burst-mode synchronization, buffering, label processing (recognition and swapping), and bit-rate conversion (compression/decompression). While many attempts have been made to implement such functions in an all-optical scheme [1]-[8], it is very difficult to make an adaptable buffer and provide highly functional packet operations such as label processing solely in the optical domain. In contrast, electrical signal processing has been successfully performed by CMOS (complementary metal-oxide-semiconductor) circuits at operating speeds below 1 GHz, but it becomes more difficult to handle optical packets by all-electrical means at higher bit-rates. To overcome this difficulty faced by all-optical and all-electrical processing schemes, NTT Photonics Laboratories is developing an optical packet processing scheme using optical serial-to-parallel and parallel-to-serial conversion, as described in the other selected papers in this issue. This scheme has the advantages of both optical and electronic devices so it can process ultrafast asynchronous burst optical packets using a low-speed but very smart CMOS circuits.

This paper reviews our recent work on ultrafast optical packet processing technologies based on this scheme. We have developed an optical label swapper, a photonic[*1] RAM (random access memory), and a packet compressor/decompressor based on our novel hybrid optoelectronic devices.

2. Optical packet processing using hybrid optoelectronics

2.1 Optical label swapping

In optical packet-switched networks, optical labels are usually updated at nodes. There have been several approaches to all-optical label swapping, using subcarrier multiplexed labels [1], [2] and serial-bit labels [3], [4]. In a subcarrier multiplexing transmission scheme, the bit-rate of the payloads must be below the subcarrier frequency to separate the label from the payload. In contrast with the serial-bit label, even if the payload bit-rate is high enough, the label bit-rate is limited and a long guard time is required due to the bandwidth of electronic label processing circuits. To solve these problems with the serial-bit label, we propose a new label swapper that can handle 40-Gbit/s 16-bit optical labels with a 1-bit (i.e., 25-ps) guard time and demonstrate the label swapping of a 40-Gbit/s optical packet with a 16-bit label and a 16-bit payload separated only by a 1-bit zero [9].

The label swapper is composed of a packet-level optical clock-pulse generator (OCG) [10], [18], an optical pulse-train generator, a 1-to-16 all-optical ser-

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ial-to-parallel converter (SPC) [11], [17], an 16-to-1 photonic parallel-to-serial converter (PSC) [12], [13], [19], and a CMOS label-swapping circuit. An asynchronous burst-mode optical packet is first launched into the OCG for packet-level synchronization. The OCG consists of a photoconductive sample-and-hold circuit, a pulse generating circuit, and a gain-switched distributed feedback laser diode. It generates a single optical pulse accurately synchronized with the leading pulse of the incoming packet. Using the pulse train from the OCG as pump pulses, the all-optical SPC performs 16-parallel conversion of the incoming packet. The parallel optical signals are converted to low-speed parallel electrical signals by a photodetector (PD) array and limiting amplifiers. The signals are then input to the CMOS circuit, which carries out the label swapping of the input parallel signal. When the label-swapped parallel electrical signals output from the CMOS circuit are retrieved, trigger signals output from the OCG are input to read 16 parallel electrical signals simultaneously from the CMOS circuit. These signals are then reconstructed into a 40-Gbit/s 16-bit optical label by the photonic PSC.

Figure 1 shows the experimental setup. The 2-ps optical pulses from a fiber laser were converted into a packet stream consisting of two alternating 40-Gbit/s 33-bit packets A (La, 0, Pa) and B (Lb, 0, Pb) at a packet rate of 42 MHz. Here, L and P represent the 16-bit label and payload, respectively (La = Pa = 1001011101010010 and Lb = Pb = 10001110011100 01), and a guard time of the 1-bit zero was inserted between the label and payload. To separate the label from the payload, part of the input packet stream was launched into an electrical pulse generator that generated an approximately 600-ps-wide optical pulse. The generator is similar to that used in the abovementioned OCG. It generated a control signal synchronized with the leading pulse of the incoming packet with a timing accuracy of better than ±2ps and with a fast rise and fall time of less than 50 ps, allowing separation within the 1-bit guard time using a 1×2 switch with a 20-GHz bandwidth (i.e., with 25-ps switching time). **Figures 2(a)**, **(b)**, and **(c)** show the waveforms of the input packets (A and B), old separated labels (La and Lb), and separated payloads (Pa and Pb), respectively. The old label and payload were successfully separated for packets A and B, with extinction ratios of 15 and 20 dB respectively. The old separated label was launched into a label swapper consisting of an OCG, an all-optical SPC, a CMOS label processing circuit, and a photonic PSC, as shown in Fig. 1. The input old 16-bit label was converted into 16 parallel low-voltage transistor-transistor-logic (LVTTL) electrical signals using the all-
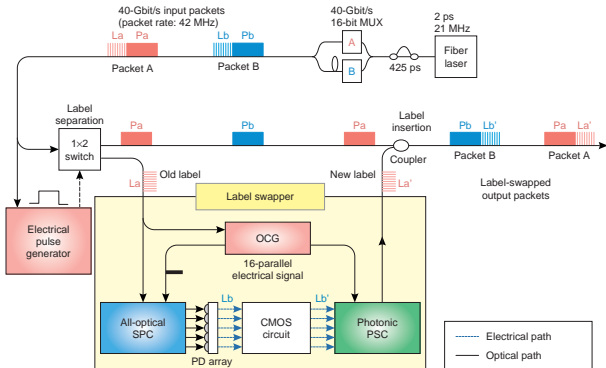

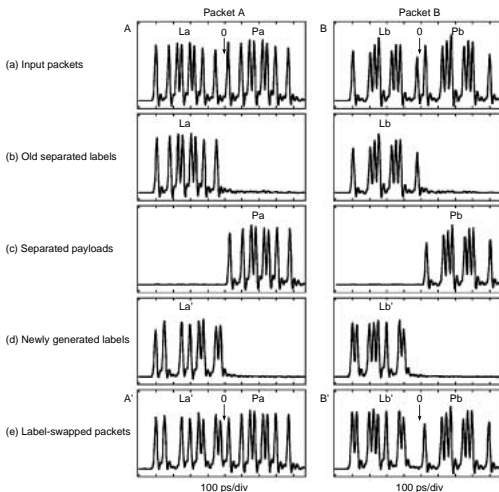Fig. 1. Experimental setup for optical label swapping.

Fig. 2. Experimental results for optical label swapping.

optical SPC and the OCG, and then input into a CMOS label processing circuit made from a field programmable gate array (FPGA). The label processing circuit included a programmable routing table consisting of many 16-bit addresses and their routing information. The input label was checked against all the addresses in the routing table simultaneously by using AND gate arrays. The circuit then decided the proper new label for the input packet and output it in the form of 16 parallel electrical signals. The 16 parallel electrical signals with the new label information were then input into the photonic PSC and converted into a new 40-Gbit/s 16-bit serial optical label. Since the new label was constructed using an optical pulse generated by the OCG, it was accurately synchronized with the separated payload passing through a constant delay line. In the experiment, the routing table was set to produce 16 channels of signals with La' = 1010001010110011 and Lb' = 1100111010011 000 for input labels La and Lb, respectively. **Figures**

2(d) and **(e)** show the waveforms of the newly generated labels (La' and Lb') and the label-swapped packets (A' and B'), respectively. The new labels were perfectly matched with the routing table, confirming that the label processing circuit successfully recognized the patterns of the two old labels, and generated the new labels according to the routing table.

2.2 Photonic RAM

Resolving packet contention is one of the most important functions for optical packet-switched networks [16]. We have proposed a photonic RAM [14] that is based on the hybrid optoelectronic packet processing scheme. The basic concept of a photonic RAM is shown in **Fig. 3**. The configuration is similar to the optical label swapper described in section 2.1. A CMOS RAM is used in place of the CMOS label-swapping circuit, and a pulse train generator (PTG) is used to store an entire packet (i.e., a header and a payload). When we use a 1-to-N SPC and an N-to-1 PSC,

the PTG generates a low-repetition optical pulse train with a period that is N times the bit interval of an input optical packet during the period of the incoming packet. Using the pulse train as pump pulses, the SPC performs N-parallel conversion of the incoming packet successively at intervals of N bits. On the other hand, when the stored packet is retrieved, trigger signals with a period of N times the bit interval of an output packet created by the PTG using a single optical pulse output from an optical pulse source are input to read N parallel electrical signals simultaneously from the CMOS RAM. The entire packet is then reconstructed by the PSC using the optical pulse train from the PTG.

When, for example, a 40-Gbit optical packet is stored in a CMOS RAM with an operating speed of 400 MHz, the packet is converted to 100 parallel signals every 100 bits with a repetition rate of 400 MHz. However, since our current SPC is limited to 16-parallel conversion, we experimentally confirmed the fundamental operation of the photonic RAM for 40-Gbit 16-bit optical packets without the PTG, as shown in **Fig. 4**. A photograph of the 40-Gbit/s 16-bit photonic RAM is shown in **Fig. 5**. It consists of an OCG, all-optical SPC, photonic PSC, and CMOS RAM. All these components are packaged in a 26 cm × 31 cm box. The CMOS RAM is made from an FPGA and is controlled by an external computer.
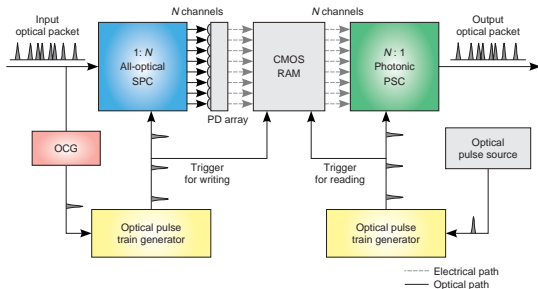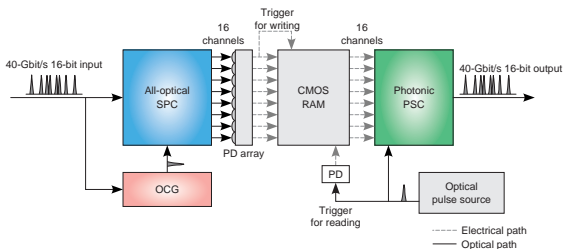

Fig. 3.   Concept of photonic RAM.

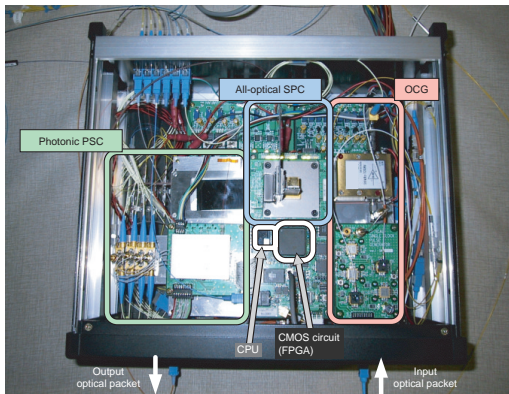Fig. 4.   Experimental diagram for 40-Gbit/s 16-bit photonic RAM.

Fig. 5. Photograph of prototype of 40-Gbit/s 16-bit photonic RAM.

A 21-MHz-repetition optical pulse train from a fiber laser (1542-nm wavelength and 2-ps pulsewidth) was converted into a 42-MHz packet stream with two alternating 40-Gbit/s 16-bit optical packets A (1001011011010010) and B (1000111001110001) using PLC-based optical multiplexers (PLC: planar-lightwave-circuit). The input optical packets were converted to parallel data using the OCG and the 1-to-16 SPC, and then stored in the CMOS RAM. The capacity of the CMOS RAM used in the present experiment was 112 kbytes because we employed a commercially available FPGA. **Figure 6(a)** shows the input packet stream with 40-Gbit/s 16-bit packets A and B. Once the optical packets had been stored in the memory, the data were preserved unless they were erased or overwritten. Therefore, we could read the stored data freely by specifying the read address using the remote computer. When all the addresses had been specified, optical packets A and B were output in turn, as shown in **Fig. 6(b)**. Meanwhile, by specifying the even addresses, we could obtain only packet A, as shown in **Fig. 6(c)**. Similarly, only packet B was output when we specified the odd addresses (not shown). The latency of the CMOS RAM is about 50 ns. The advantages of the photonic RAM are summarized in [16].

2.3 Optical packet compressor/decompressor

As the bit-rate of high-performance backbone networks greatly surpasses that of cost-effective and flexible metropolitan networks, the compression and decompression of burst optical packets will be the key technology for edge routers that connect backbone and metropolitan networks. The simultaneous conversion of the output spectral width that corresponds to their bit rate is also a desirable function for effective wavelength utilization in future WDM-based large-capacity packet-switched networks (WDM: wavelength division multiplexing). Recently, optical packet compression and/or decompression have been demonstrated using a fiber delay line lattice [5], [6] or a fiber delay loop [7], [8] which are based on the bit-by-bit feed-forward control of an input packet using optical delay lines with 2×2 switches. Therefore, it is difficult to handle a long optical packet (more than about 10 bits) because a long optical delay line that corresponds to the optical packet is necessary for compression and/or decompression and to convert the spectral width of an output packet. For example, for a 40-to-10-Gbit/s decompression of an optical packet with a return-to-zero format, the spectral bandwidth of the output packets remains 40 GHz in spite of their reduced bit-
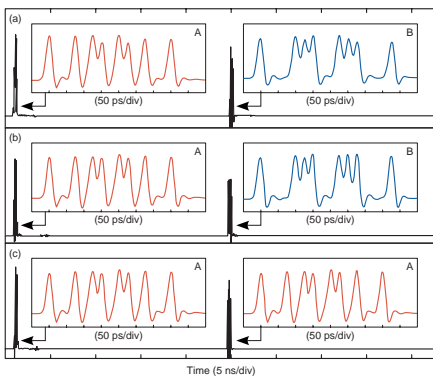
Fig. 6.   Experimental results for address-specified readout. (a) Input packets A and B. Output packets when (b) all addresses were specified and (c) only even addresses were specified.

rate at 10 Gbit/s. To meet such a requirement, we propose a novel compressor/decompressor and demonstrate compression and decompression for 40-Gbit/s 32-bit optical packets [15].

Figure 7 is a schematic diagram of our system. This system has the same configuration as a photonic RAM except that it uses a 32-bit all-optical SPC and a 32-bit photonic PSC. The 32-bit SPC (PSC) is composed of two 16-bit SPCs (PSCs). For generating original 40-Gbit/s 32-bit packets, the data output from the CMOS circuit are bundled into four groups of four bits each. Each group is passed to a 4:1 electrical PSC circuit, which generates a 10-Gbit/s, 4-bit serial electrical signal. This serial signal drives an electroabsorption modulator (EAM), which modulates a 10-Gbit/s 4-bit optical pulse train generated by an optical multiplexer. The four modulated signals are interleaved with a bit separation of 25 ps, resulting in a 40-Gbit/s, 16-bit optical packet. Then, by using two 16-bit PSCs, the second 16-bit output packet is forwarded after the first one to make a 40-Gbit/s 32-bit optical packet. We can achieve packet compression and decompression simply by changing the length of the delay lines after the EAMs and the arrangement of the 32-channel data from the CMOS memory using an external computer. **Table 1** lists three examples of bundled groups of 32-bit data launched into eight electrical PSCs, and **Fig. 8** shows

Table 1.   Bundled groups of data in 32-bit optical packet.

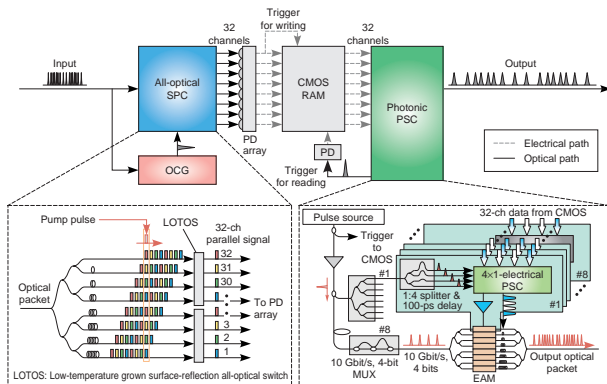| PSC	Example 1 (40-Gbit/s output)	Example 2 (80-Gbit/s output)	Example 3 (10-Gbit/s output)
#1	1, 5, 9, 13	1, 9, 17, 25	1, 2, 3, 4
#2	2, 6, 10, 14	2, 10, 18, 26	5, 6, 7, 8
#3	3, 7, 11, 15	3, 11, 19, 27	9, 10, 11, 12
#4	4, 8, 12, 16	4, 12, 20, 28	13, 14, 15, 16
#5	17, 21, 25, 29	5, 13, 21, 29	17, 18, 19, 20
#6	18, 22, 26, 30	6, 14, 22, 30	21, 22, 23, 24
#7	19, 23, 27, 31	7, 15, 23, 31	25, 26, 27, 28
#8	20, 24, 28, 32	8, 16, 24, 32	29, 30, 31, 32

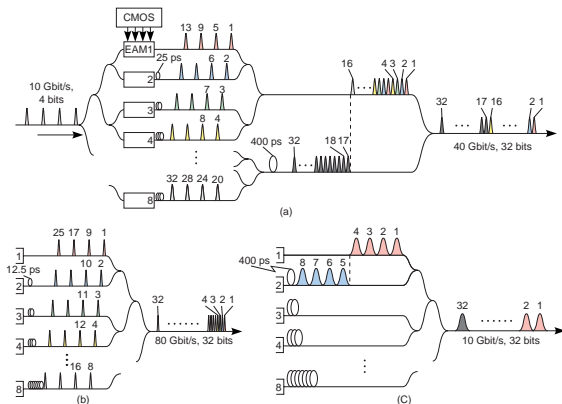Fig. 7. Principle of 32-bit optical packet compressor/decompressor.

Fig. 8. Relationships among the groups of the data number and arrangement of eight 10-Gbit/s 4-bit optical packets when generating (a) 40-Gbit/s, (b) 80-Gbit/s, and (c) 10-Gbit/s output packets, respectively.

relationships among the groups of the data number and arrangement of eight 10-Gbit/s 4-bit optical packets. As shown in Fig. 8(a), when the data are bundled in the groups of Example 1 and the eight 10-Gbit/s 4-bit optical signals through the EAMs are interleaved with a bit separation of 25 ps, a 40-Gbit/s 32-bit optical packet is output with the same bit rate as the input packet. Meanwhile, when the data are rearranged as in Example 2 and the eight optical signals through the EAM are interleaved with a bit separation of 12.5 ps, the optical packet can be compressed to 80 Gbit/s, as shown in Fig. 8(b). In contrast, if we use the data groups of Example 3 and forward the 4-bit optical signals successively through delay lines that differ by 400 ps, the packet can be decompressed to 10 Gbit/s, as shown in Fig. 8(c).

In the experiment, 1542.2-nm 7.5-ps optical pulses from a fiber laser with a repetition rate of 21 MHz were split into two and converted into different 40-Gbit/s 32-bit optical packets A (10010101101001011 001011011010010) and B (10001110011100011000 111001110001) using PLC-based optical multiplexers. By interleaving them with each other, we created an input optical packet stream at a packet rate of about 42 MHz. The pulses were launched into the system and stored in a CMOS memory made from an FPGA. The latency of the CMOS memory used in this experiment was about 80 ns. To demonstrate packet compression and decompression, we prepared three optical pulse sources with different pulsewidths and center wavelengths for the photonic PSC (42-MHz repetition rate): 3.0 ps at 1543.6 nm for 80-Gbit/s output, 7.5 ps at 1543.8 nm for 40 Gbit/s, and 30 ps at 1572.9 nm for 10 Gbit/s. We measured the 80-Gbit/s waveforms using a cross correlator with a 2.0-ps reference pulse and measured the others using a sampling oscilloscope with a 3-dB bandwidth of 65 GHz. **Figure 9** shows the experimental results we obtained for the packet compression and decompression of 40-Gbit/s 32-bit optical packets. By changing
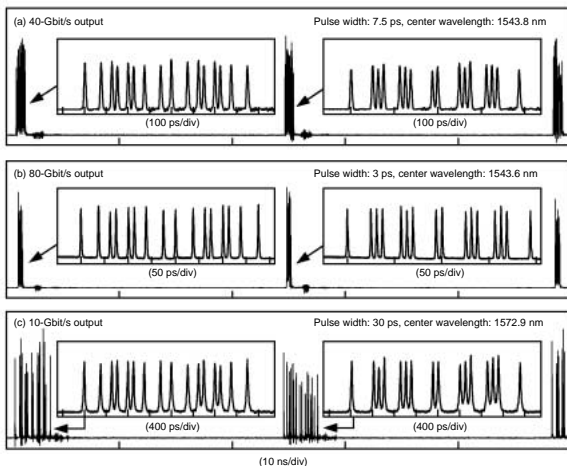

Fig. 9. Reconstructed output optical packets from optical packet compressor/decompressor with bit-rates of (a) 40 Gbit/s, (b) 80 Gbit/s, and (c) 10 Gbit/s.

the data arrangement, the delay lines after the EAMs, and the optical pulse source of the photonic PSC as mentioned above, we successfully reconstructed 32-bit packets with three different bit rates, pulsewidths and center wavelengths: (a) the original 40 Gbit/s packets, (b) compression to 80 Gbit/s, and (c) decompression to 10 Gbit/s. Note that our system can easily cope with other output bit rates by changing the output bit-rate of the 4-bit signal from the electrical PSC circuit and delays in the optical multiplexer that generates the 4-bit optical pulse train; it can cope with other input bit-rates by changing the delays in the all-optical SPC.

3. Conclusion

We have described our approach to the ultrafast optical packet processing technologies required for future optical packet-switched networks, namely a label swapper, a photonic RAM, and a packet compressor/decompressor. These are key components of a system, based on an OCG, all-optical SPCs, and photonic PSCs, that enables highly functional processing by using smart CMOS circuits that consume little power for 40-Gbit/s asynchronous burst optical packets. In addition, they feature scalability of the number of bits, compatibility with other electronic circuits, and compactness. Further advances in ultrafast optical packet processing technology will greatly contribute to the construction of future optical packet-switched networks.

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