1.25-Gbit/s Burst-Mode Receiver ICs with Quick Response for Passive Optical Network Systems

Makoto Nakamura†, Yohtaro Umeda, Jun Endo, and Yuji Akatsu

Abstract

We have developed burst-mode receiver integrated circuits (ICs) with a quick response for 1.25-Gbit/s passive optical network systems. In such a system, the receiver should be able to handle burst-data packets. We have devised a transimpedance amplifier with three gain modes that uses hysteresis comparators and a limiting amplifier with feed-forward auto-offset control. Using these design techniques, receiver ICs were fabricated using silicon germanium bipolar complementary metal oxide semiconductor (SiGe-BiCMOS) technology. The receiver exhibits a fast settling time of under 44 bits and sensitivity of –30 dBm using a PIN-photodiode (positive-intrinsic-negative photodiode (PIN-PD)) at 1.25 Gbit/s. The use of a conventional PIN-PD and the freedom from external adjustment make it possible to build an inexpensive receiver.

1. Introduction

Communication traffic, which includes both voice and image data, is growing rapidly as Internet use expands. To provide broadband communications, a high-speed access network like fiber-to-the-home is desired. A passive-optical-network (PON) optical-subscriber system is inexpensive because it provides point-to-multipoint communication and has big advantages in both data transfer speed and cost [1], [2]. The speed has been steadily increased as we have progressed from the synchronous-transfer-mode (STM) PON through the asynchronous-transfer-mode (ATM) PON and broadband PON [3] to reach the gigabit-class PON [4], [5].

A PON system and the burst-mode optical receiver used in it are shown in **Fig. 1**. A passive optical coupler allows several optical network units (ONUs) to share an expensive optical line terminal (OLT), which decreases the cost of the optical access system. On the other hand, such a shared-access system has a large path loss due to the large number of ONU branches. Upstream and downstream data using the optical wavelengths of 1.31 and 1.49 μm, respectively, is multiplexed by a wavelength division multiplexer (WDM). In the downstream traffic, data packets are transmitted continuously with uniform amplitude. In contrast, burst-data packets in the upstream traffic are transmitted with very different power levels because of the different transmission distances between the ONUs and the OLT. The OLT must be able to handle this irregular upstream data. Hence, the optical receiver in the OLT is a key component of a PON system.

The receiver in the OLT consists of a photodetector (e.g., a photodiode (PD)) and an amplifier, as shown in Fig. 1. The PD converts received optical signals to electrical ones, and the amplifier amplifies the signals to a sufficient amplitude for the signal-processing large-scale integration (LSI) chip to handle. The performance requirements for the optical receiver in a gigabit-class PON system are shown in **Fig. 2**. Because a passive optical coupler is used, the signals are branched off and the shared-access loss is large. To compensate for this shared loss, the receiver should have a high sensitivity and a wide dynamic range for the input signal power that can be accommodated. Moreover, in a PON system, each packet

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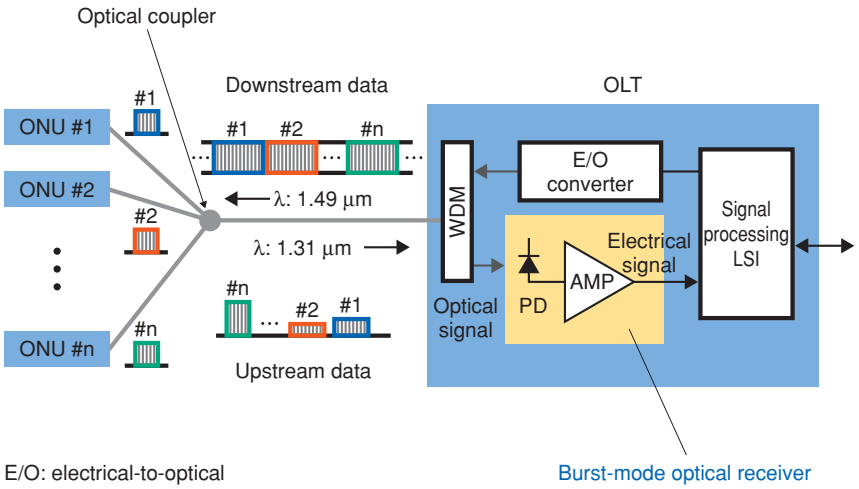

Fig. 1. PON system and an optical receiver for an OLT.

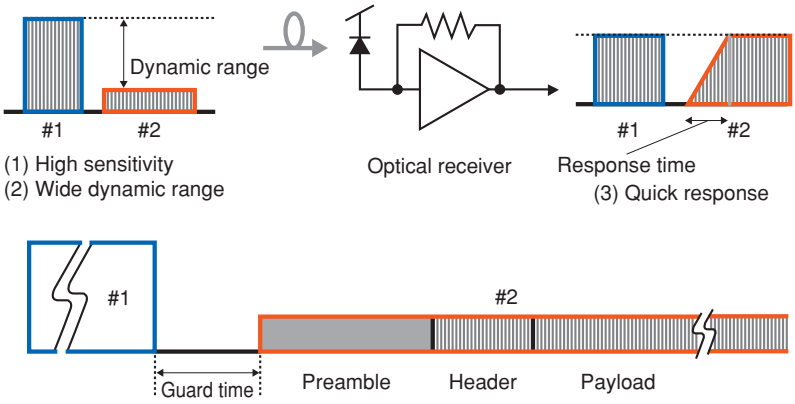

Fig. 2. Performance requirements for the optical receiver.

consists of a preamble, a header, and a payload, and the receiver's settling time must be less than the preamble time. If we can shorten the response time, we can reduce the preamble time and thereby improve the efficiency of uplink-data transmission [6]. Moreover, for access networks, the cost of the receiver must be low enough for subscriber use. However, the OLT receivers in gigabit-class PONs generally use an expensive avalanche photodiode (APD) as the photodetector to obtain high sensitivity [7]. The problems with conventional receivers are summarized in **Table 1** along with our design targets.

To meet these requirements, we have devised circuit design techniques that enable both a quick response and high sensitivity using an inexpensive positive-intrinsic-negative photodiode (PIN-PD) [8], [9].

Table 1. Properties of conventional receivers and our targets.

	Conventional values		Target values
Photodetector	APD	PIN-PD	PIN-PD
Sensitivity	High (< –30 dBm)	Low (–26 dBm)	High (< –30 dBm)
Gain control	O/E conv. gain	Trans-Z gain	Trans-Z gain
Response speed	Slow (μs)	Slow (μs)	Fast (<35 ns)
Supply voltage for PD	High voltage	VCC common	VCC common
Cost	High	Low	Low

Trans-Z: transimpedance

2. Circuit design techniques for a burst-mode optical receiver

The developed burst-mode optical receiver consists of a transimpedance amplifier (TIA) and a limiting amplifier integrated circuit (IC), as shown in **Fig. 3**.

2.1 TIA circuit

For high sensitivity and a wide dynamic range, we used a TIA with variable-transimpedance gain. A detailed circuit block diagram of the new TIA is shown in **Fig. 4**. The TIA consists of an amplifier core with a variable-feedback resistor R_f controlled by means of a quick level-detection circuit, a single-to-balance converter, and an output buffer. The level-detection circuit is configured using comparators with hysteresis characteristics.

The operating principle of the gain-mode switching is shown in **Fig. 5**. The TIA has three gain modes: high, medium, and low. When the input signal is small, a high feedback resistance value R_H is selected to decrease thermal noise and thereby obtain high

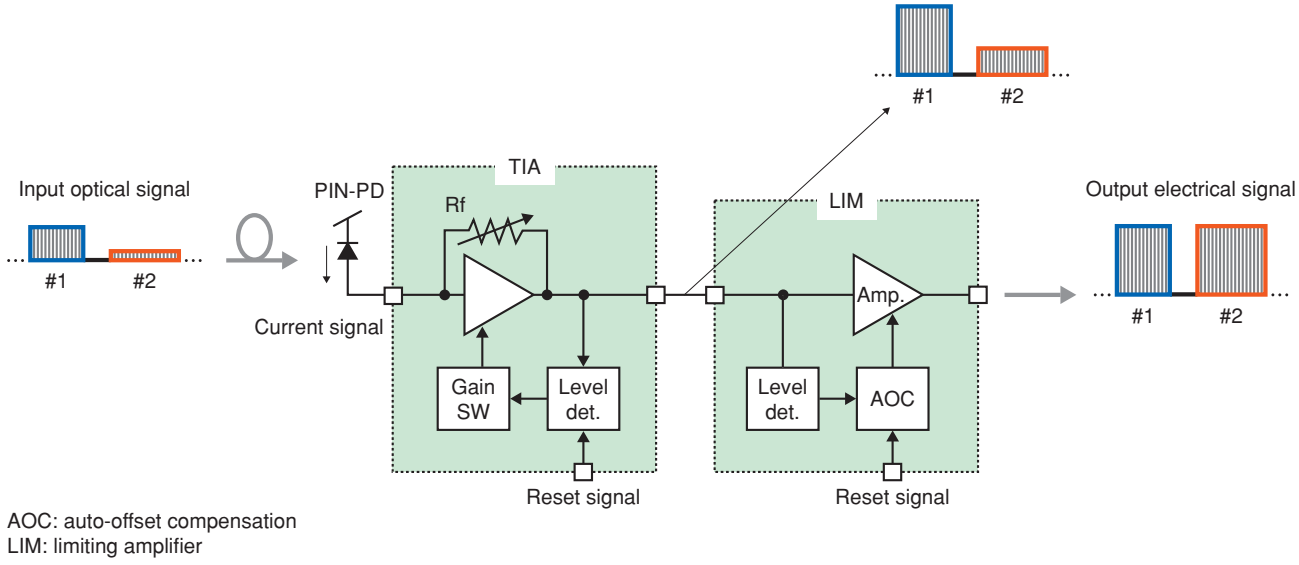

Fig. 3. Optical receiver circuit configuration.

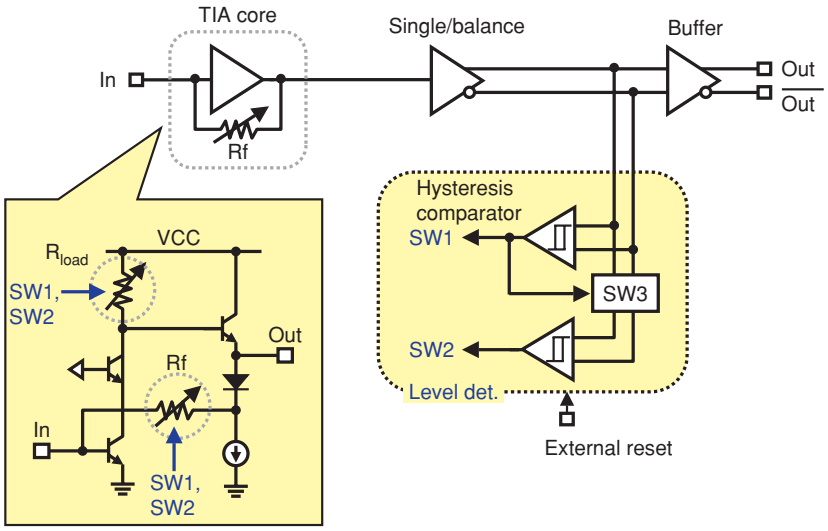

Fig. 4. TIA circuit diagram.

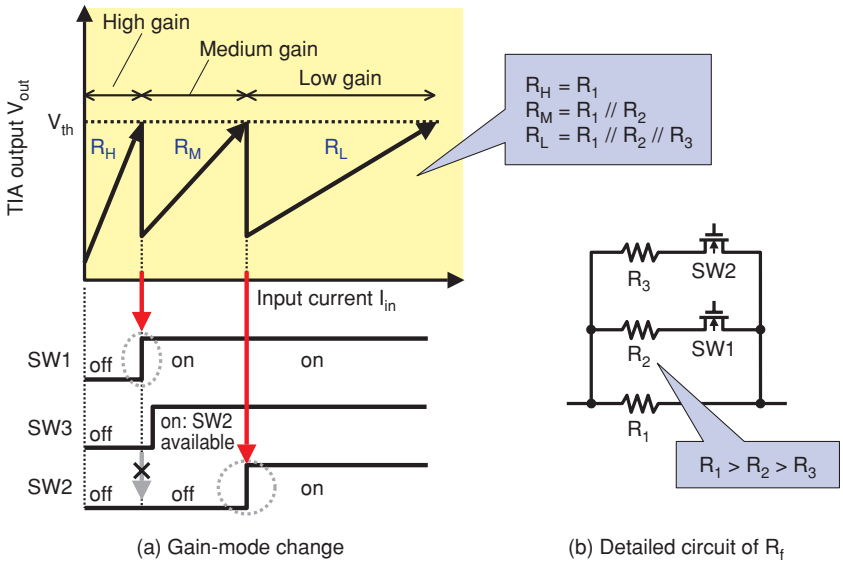

Fig. 5. Principle of gain-mode change in the TIA.

sensitivity. If the input signal current is large, the value of the feedback resistor is reduced to R_M or R_L to avoid waveform degradation. To change the gain mode, when the amplitude of the output voltage of the TIA reaches the threshold voltage (V_{th}), switch *SW1* turns on and initiates the first change from high to medium. After *SW1* turns on, *SW2* becomes available through *SW3*, which is controlled by *SW1*. The second gain mode change, from medium to low, is performed by *SW2*. The detailed circuit of the feedback resistor R_f is shown in Fig. 5(b). The feedback resistor R_f, which can take three values: R_H, R_M, and R_L, contains three separate resistors: a large one R_1, a medium one R_2, and a small one R_3. It is controlled by the level-detection circuit. R_2 and R_3 are connected to R_1 in parallel using metal oxide semiconductor field effect transistor (MOSFET) switches, which are controlled to change the gain mode.

Fast response is also essential for burst-mode operation. The response speed of the level detection and switching mainly determines the speed of the gain-mode change. For high-speed detection, we use a hysteresis comparator, which enables fast level detection and hold. Once the input signal exceeds the hysteresis voltage of the comparator V_{th}, the output is quickly changed to on. And the level of the detected signal is maintained due to the hysteresis transfer characteristics. This means that the TIA can quickly switch the gain without any external adjustments.

2.2 Limiting amplifier circuit

For burst-mode operation, the receiver should be able to handle data packets with different amplitudes corresponding to the various transmission distances. To handle these data packets, the offset voltage in each data packet should be eliminated to generate a clear reshaping signal that can be received in the following digital circuits. The offset voltage gives rise to duty cycle variation of the signal and degrades the receiver performance. To remove the offset due to packet data, we used a limiting amplifier with an auto-offset compensation (AOC) circuit.

A circuit block diagram of the limiting amplifier and an outline of the AOC operation are shown in **Fig. 6**. For accurate compensation, we used a two-stage amplifier with a feed-forward AOC [9] configuration that performs coarse and fine offset compensations. In a conventional limiting amplifier, AOC uses a feedback loop configuration for stable operation. However, the feedback loop takes a long time to respond to any change in offset conditions. On the other hand, the feed-forward configuration provides a quick response because there is no feedback loop.

In addition, to improve the accuracy and dynamic range of the offset compensation, we used a two-stage AOC configuration. When the input signal is small, coarse AOC is performed in the first-stage AOC circuit and fine AOC is performed in the second stage. When the input signal is large, the offset voltage is effectively cancelled in the first-stage AOC circuit. In addition, this AOC circuit enables high sensi-

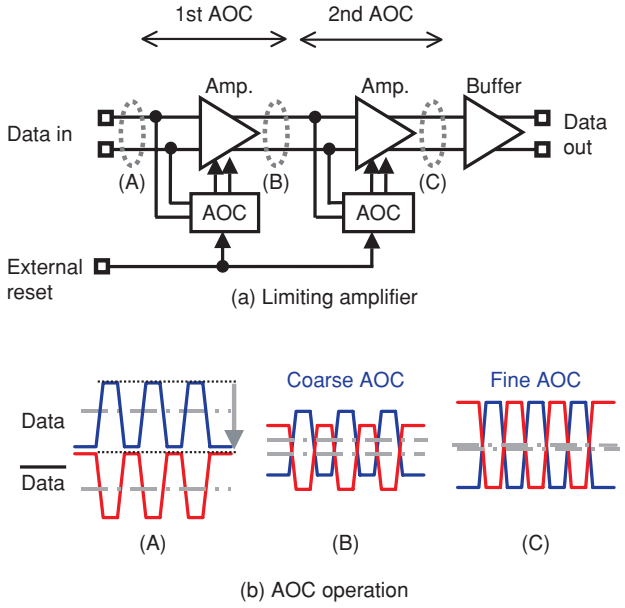

Fig. 6. Limiting amplifier circuit diagram and AOC operation.

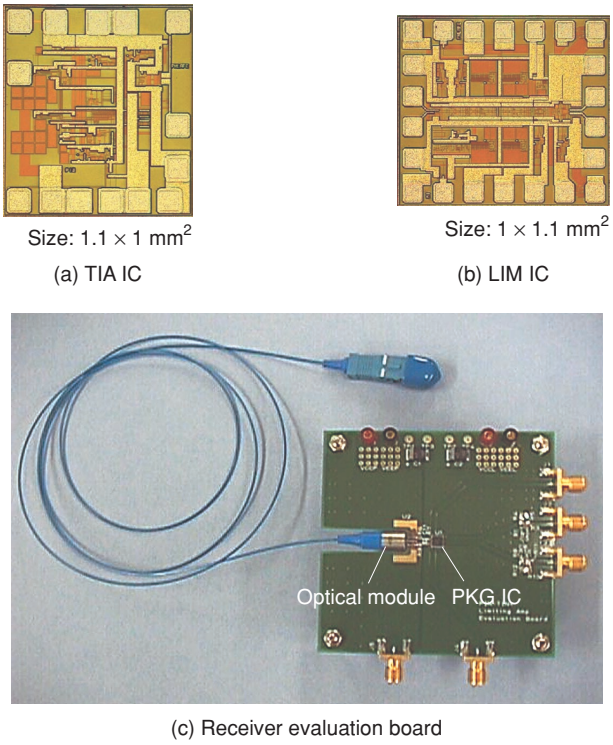

Fig. 7. Optical receiver ICs and the evaluation board.

tivity without any external adjustments because the two-stage configuration mitigates the accuracy requirement in the level-hold operation. In this circuit, a reset signal initializes the condition of offset compensation for each packet. These circuit techniques enable a quick response.

For stable operation at a data rate of 1.25 Gbit/s, a differential interface with 50-Ω impedance matching was used between the TIA and limiting amplifier circuits. The electrical output interface of the limiting amplifier is differential low-voltage positive emitter-coupled logic (LVPECL). Consequently, the circuit techniques used in the TIA and limiting amplifier enable the receiver's settling time to be very short and enable data to be output with a constant amplitude.

3. Experimental results

3.1 IC fabrication

Using these circuit design techniques, we fabricated TIA and limiting amplifier ICs using silicon germanium bipolar complementary metal oxide semiconductor (SiGe-BiCMOS) technology. Microphotographs of the ICs are shown in **Figs. 7(a)** and **(b)**, respectively. The die sizes are 1.1 mm × 1.0 mm for the TIA IC and 1.0 mm × 1.1 mm for the limiting amplifier IC.

The TIA IC with a PIN-PD was packaged in a conventional metal can, and the limiting amplifier IC was molded in a low-cost plastic package. An optical receiver was built using this optical module and the packaged limiting amplifier IC. A photograph of the evaluation board of the receiver is shown in **Fig. 7(c)**. The supply voltage of the optical receiver is +3.3 V and the power dissipation of the ICs is about 300 mW, excluding the output load current.

3.2 IC performance

The receiver was operated at 1.25 Gbit/s and the performance was evaluated using burst-mode optical data with a pseudo-random-bit sequence (PRBS). Waveforms for high-, medium-, and low-gain modes at optical input powers of –30, –24, and –10 dBm, respectively, with an extinction ratio of 10 dB are shown in **Fig. 8(a)**. These results confirm that the receiver could generate data with clear eye opening in all gain modes. Even in the high gain mode, a clear eye pattern was obtained for a small optical input signal of –30 dBm. Our circuit techniques make it possible to improve the sensitivity compared with conventional ones [6], [10], [11]. The measurement results reveal that the sensitivity of the developed

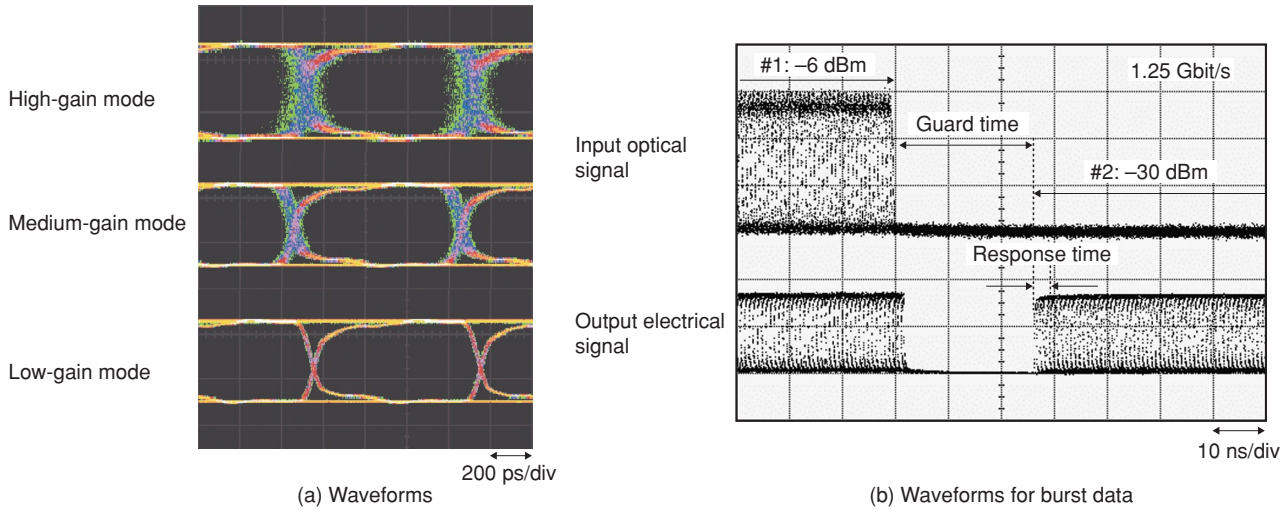

Fig. 8. Response waveforms of the optical receiver ICs.

receiver with a PIN-PD is as high as that of one with an APD for burst-mode use [7].

To demonstrate the response speed, we evaluated the response waveform for burst data. An example of the receiver output waveforms for packet data with different amplitudes is shown in **Fig. 8(b)**. The top waveform is an optical input, and the bottom one is the receiver output. The optical power of the first packet was –6 dBm and that of the second one was –30 dBm. The receiver generated a clear reshaped signal with constant amplitude. The output waveform also shows that the settling time for the second packet was very short. These results show that the receiver can respond quickly to burst data and generate a constant output amplitude for extremely different input optical powers.

We also evaluated the response speed taking into consideration gain-mode switching. The responses to burst data in bit-error-rate measurements in the high-, medium-, and low-gain modes are shown in **Fig. 9**. In this figure, the horizontal axis is the starting bit of error counts in packet data, or the settling time. The receiver achieved a fast settling time of under 44 bits, which satisfies the specifications for both GE-PON (Gigabit Ethernet PON) [4] and G-PON (Gigabit PON) [5].

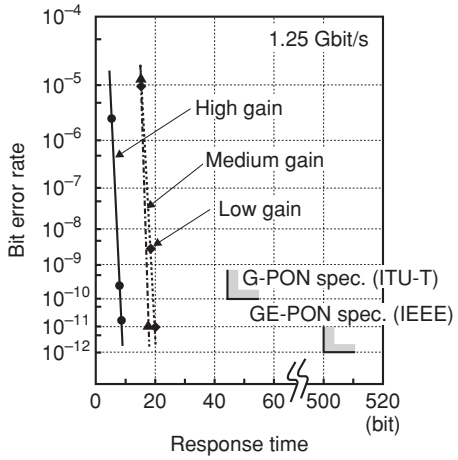

Fig. 9. Response to burst data in bit error rate.

4. Conclusion

Burst-mode optical receiver ICs with a quick response for gigabit-class PON systems have been developed. To achieve a quick response and high sensitivity at the same time, we devised a TIA circuit with three gain modes that uses hysteresis comparators and a limiting amplifier circuit with feed-forward AOC. Using these design techniques, we fabricated burst-mode receiver ICs. An optical receiver built with these ICs and a PIN-PD exhibited a quick response and high sensitivity for burst data. Its sensitivity is comparable to that of a receiver with an APD. Furthermore, the performance is good enough to satisfy the GE-PON and G-PON specifications. Therefore, these fast-response burst-mode receiver ICs will be very useful in improving the transmission efficiency of burst-mode optical communications systems. These receiver ICs have been implemented in an optical transceiver, as described in the next paper in this issue [12].

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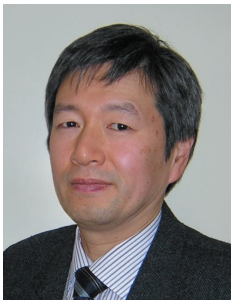

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