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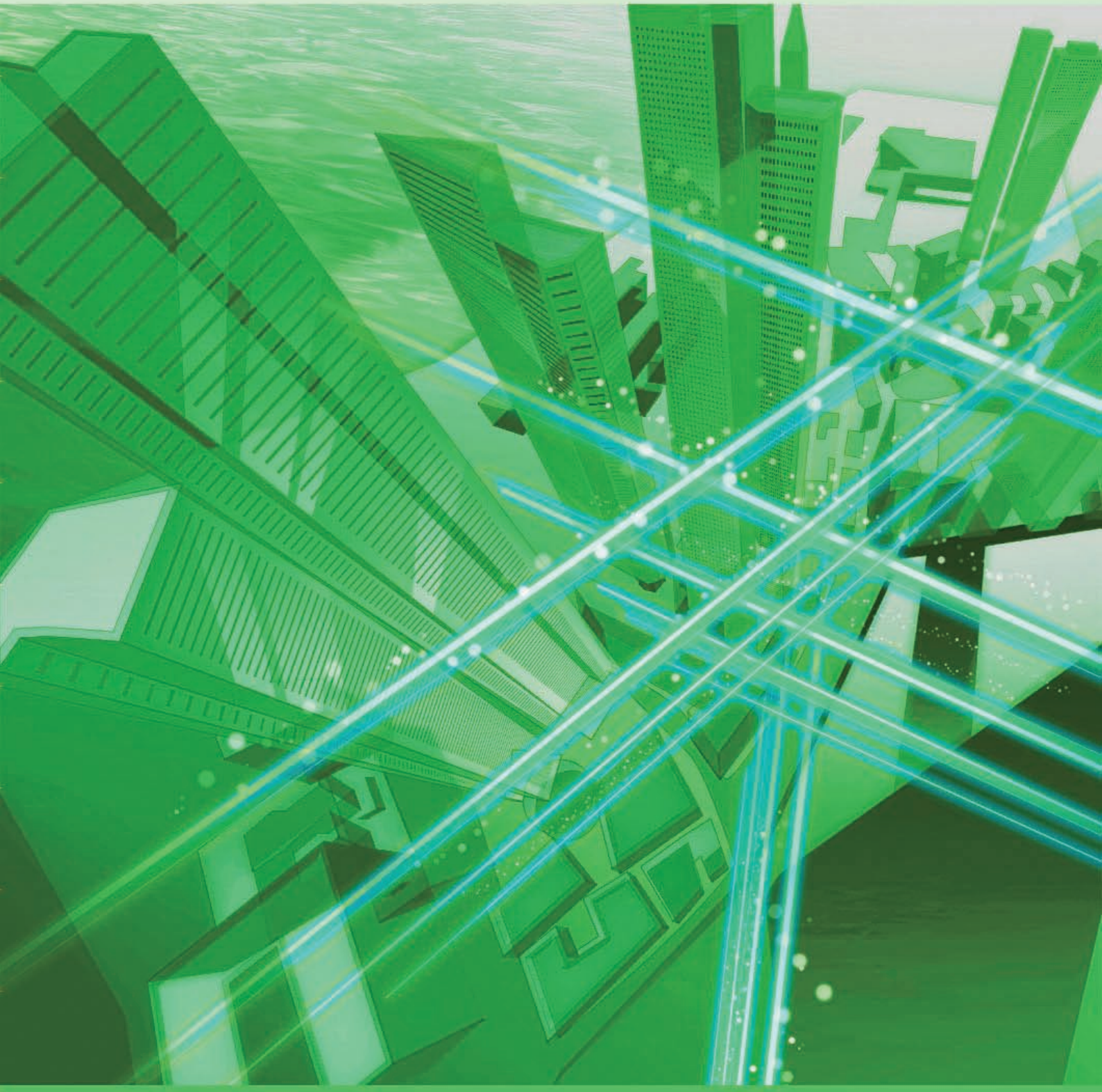

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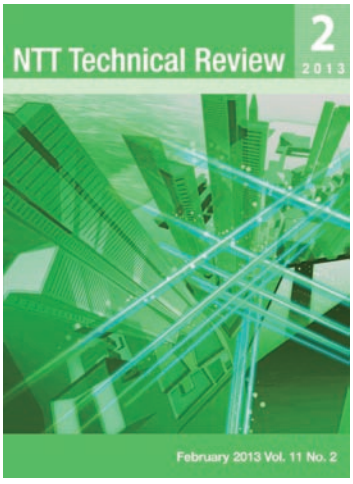


Keeping Up the Challenge in a Turbulent Market —Moving from Self-sufficiency to Maximum Use of Alliances

Kazutoshi Murao
President of NTT WEST

Overview

What strategies should be adopted to face the very severe conditions of the current telecommunications market? Kazutoshi Murao, President of NTT WEST, says that the NTT WEST Group must adopt a "one step forward" attitude to get back on the path to growth. We asked him about the future direction of NTT WEST and the strategies it needs to adopt.

The key to healthy sales and profits is helping to create and design a new communication culture and lifestyle

—Mr. Murao, it's been about half a year since you became president of NTT WEST. Do you feel that you have settled into your new position? Please tell us about your aspirations and growth strategies looking forward.

At the time of my appointment, I was overflowing with ideas, and all I could think about was ways of implementing them. But on assuming this office, I didn't have nearly as much time for detailed and thorough strategic planning that I thought I'd have. Nevertheless, I want NTT WEST to become a "culture-creation company," and I would like all of us in the NTT WEST Group to bring a lot of spirit and energy to our work in line with this corporate direction.

Let me be more specific. First, in the face of decreasing revenues in voice-related services and increasing revenues in Internet protocol (IP)-related services, I plan to do everything in my power to eliminate this revenue gap between two business areas that are said to be uncomplementary. I will also promote service development and the creation of alliance-type services based on a mindset that places importance on improving our customers' lifestyles. This is how I plan to establish a stable financial foundation for NTT WEST.

On the whole, there are about 16 million subscribers to telephone services and about 7 million subscribers to optical—or HIKARI—broadband services at NTT WEST. If we can raise the average revenue per user by providing additional optical fiber services, we may be able to increase revenues by 20–30 billion yen. In this way, I would like to close the revenue gap that I just mentioned at an early date and increase our overall revenues.

At present, the longtime growth in optical broadband services is starting to slow down as mobile services using smartphones, tablets and other mobile devices continue to spread. Under these conditions, I would like to position Wi-Fi as a bridge between optical and mobile services and to aggressively develop services that make use of Wi-Fi.

Of course, we will also be focusing our efforts on cloud-related businesses. We have set up a development and strategy-planning system for cloud

businesses and have expanded our support staff to 500 employees. By doing so, we hope to change our traditional corporate business style to a sales style centered on the cloud.

As we look forward, we will make an all-out effort to create new services. In this endeavor, it is important that we design new services from the viewpoint of customer lifestyle.

Moving from self-sufficiency to maximum use of alliances

—Please tell us something about alliance-type businesses.

While I would like to see all NTT WEST employees working together on projects for developing new optical fiber services, I would also like to see us becoming even more active in the development of alliance-type businesses as part of this effort. Instead of adhering to an extreme belief in self-sufficiency, we need to consider that forming alliances with companies possessing world-class technologies, extensive know-how, and advanced networks can lead to prompt creation of novel services that can help create a new communication culture and lifestyle.

To this end, we have established an alliance promotion office and have set out to form alliances focused mainly on video services such as Smart TV. Perhaps the announcement of our recent partnership with Hulu, the online video delivery service, is still fresh in your minds. From here on, I plan to form various alliances in order to make compelling services like Smart TV a reality.

We have also set up a business-design promotion office and a cloud business department. Our aim here is to create highly novel businesses. We want to design and implement models for unconventional, progressive businesses and services without being restricted to telecommunication services by collaborating with business operators in a variety of fields.

For example, we have established a company called NTT SMILE ENERGY together with OMRON Corporation to provide energy-saving support services for households. These services include providing users with the technology to visualize their energy savings and electric power usage and generation. We have also begun to develop cloud services for health management in collaboration with hospitals and public welfare services together with local governments. Additionally, we have partnered with Yamaha Corporation to provide a service that enables musicians in different locations to perform together using *Hikari Denwa*, our optical-fiber IP phone service, without feeling a delay. If we tried to develop novel services like these entirely on our own, I don't think we'd be able to create a new communication culture.

In the beginning, I think our employees were somewhat at a loss as to how to go about forming such alliances, but now, they are quite happy to hop around the country looking for strategic partners.

Up to now, we have been involved with a variety of undertakings centered on the construction of the Next Generation Network. However, focusing only on the network will not enable us to keep up with the times. In the end, it is essential that we change our way of thinking and take up projects in tune with the aspirations of our customers and alliance partners if we are to be accepted by society as a viable player.

In addition, statistics show that mobile phones are more likely to be used indoors, inside the home. With this in mind, we are providing a service called "Sumaho De Hikari Denwa" that enables a smartphone to be used as an extension of the Hikari Denwa service in the home, thereby drastically reducing calling charges. This service was made possible by an application that was developed by a small venture company in Kyoto that had been working out of a small apartment in a condominium building. We have been able to form alliances with such companies and provide services that please our customers, but it is not easy to determine exactly where such chances lie. For this reason, it is important for us to venture out beyond the confines of the company and work up a sweat, so to speak, visiting customer sites to keep us wired into the needs of society. We must change our behavior patterns, and that includes me as well.

Clients are great business partners

We have found our customers to be great business partners. It is my desire to treat our customers as highly valued clients, and at the same time, to become a valuable business partner to our customers. I want to establish new and exciting businesses that combine the strengths of our customers with our advanced ICT (information and communications technology) platform.

To this end, I would like to see our sales staff—which has many opportunities to interact with our customers—serve as "troops" on the lookout for business opportunities that we call "seeds." My plan is to set up, by summer, a department in each region of the country to search out opportunities to form alliances. You can expect these troops to promote alliance-type businesses not just from the viewpoint of selling something but also with the goal of discovering the seeds of future business.

Responding to difficult times in an attack pose with spirit and joy

—Market conditions for the entire industry are considered to be very severe. How do you confront this battle for market share?

In my mind, we must always keep up the attack in the market share battle with a firm resolution to succeed; losing is not an option. We are continuing to move forward in this battle, but the management environment and the broadband industry are undergoing tremendous changes. If we fail to realize that optical fiber is not the center of broadband services, we will truly be left behind. Players from around the world with a focus on smartphones and other mobile devices are entering network-related businesses bringing about drastic changes at an unimaginable speed.

Despite these changes, there are companies that are happily moving forward and achieving good results. It is not a good thing that the company managers use the word "severe." It can be said that the so-called "severe" conditions are simply a call for spirited action—it will not help to simply give up and become complacent about those conditions.

In other words, because the changes are as dramatic as those that occurred during the Meiji Restoration, it is exactly during turbulent times like these that we should be excited about moving forward and taking up the challenge of building a better world. From a global viewpoint, NTT WEST is just another enterprise among many, but I believe that being conscious of where we stand and taking necessary measures can put us on the path to success.

During my 30s and 40s, I had the good fortune to work under some senior personnel with strong personalities who trained me well. Learning from them, I became convinced during my years as a branch general manager that "seeds are found in the field, at the front line." This is why I always made the rounds of local sites by myself. If I were to make these rounds with a retinue of assistants, those sites would be informed beforehand of my visit and would "clean up" accordingly, preventing me from seeing how they operated on an everyday basis. At first, employees complained that they could not "emotionally prepare" for my visit, but they gradually became accustomed to my impromptu appearances and to talking to me about work conditions and problem areas. The true state of conditions in the field holds abundant ideas for improving business.

This approach holds true for corporate business too. In analyzing the frequent occurrence of certain types of problems, I found that personnel in charge would often keep the problems to themselves and fail to consult with their superior. No doubt they thought that openness in the workplace was not such a good idea and feared a reprimand from their superior. To improve this situation, I told those holding positions of responsibility that "The worse the news is, the sooner it should be reported. Good news can be sum-

marized later, say in written reports." I could then take action in dealing with such problems and even go out to the site in question.

Consequently, as a branch manager, I was often asked to travel to sites to partake with personnel in negotiations with customers, and this sometimes meant driving more than 100 kilometers in one day. Through those experiences, I couldn't help but find the work to be interesting and enjoyable".

I still follow this management style taught to me by my superiors. I consider it to be my roots.

Intuition, decision, and heart

—Mr. Murao, can you leave us with a few words for NTT WEST employees?

My personal motto, which I learned from the president of a certain bank during my days as a branch manager, is "intuition, decision, and heart." This is short for "exercising your intuition, making a decision, and unifying the hearts of the people under you." A top executive must be able to make projections about the near future and to read "forward-looking vectors," and to then make decisions as a matter of responsibility. Most competent executives possess these qualities. The most important quality of all, however, is being able to unify the hearts and minds of the company's employees. Failure to do so can lead to accusations of "power harassment" and a reputation as a dictator. To be sure, this is not an easy task, but if a manager is not up to it, there is no way of moving the organization forward.

To this end, I use an "indirect circuit," in which I make an effort to study reports not just from sections in charge of key areas but from other sections as well. I believe that I can spot things from a slightly indirect view that I would not notice from a point within the "whirlpool" of activity. I place a great deal of importance on this approach, which leads to various opportunities for having detailed talks with employees.

And here, I mean all employees. There is no reason to give the executive staff special attention—they are also "colleagues" to one and all within the company.

If I were to be revered with calls of "President!" and paraded around like a *mikoshi* or portable shrine on the shoulders of others, the end would certainly be in sight for me. There are no "distinguished" personnel at NTT WEST as far as I'm concerned. To everyone, I say, "Let's move forward as one."

—And finally, can you leave a message for NTT researchers?

As a researcher, there are fields that one would like to pursue and make achievements in. But from a business point of view, it's important that such research desires be skillfully matched up with management goals. Failure to achieve such a match can only lead to misunderstandings. I'm not saying that we have so far not been achieving mutual understanding, but I would like to create an atmosphere that makes it even easier to understand each other's needs and to convey one's true feelings so that we can exchange opinions more effectively. To facilitate intensive discussions, the topics should be narrowed down, and honest, in-depth debates should be pursued. Discussions of this type can help us move forward with a sense of urgency completely in line with the company's direction.

Interviewee profile

■ Career highlights

Kazutoshi Murao entered Nippon Telegraph and Telephone Public Corporation in 1976. After serving as News Release Manager and Secretariat Manager in the NTT Public Relations Office, he became General Manager of the NTT WEST Kyoto Branch in 2000, NTT WEST Senior Vice President and Managing Director of the Corporate Strategy Planning Department in 2005, and Executive Vice President and Managing Director of the Corporate Strategy Planning Department in 2008. He became Senior Executive Vice President in 2009 and assumed his present position in June 2012.

Device Innovations toward the *Green* of Information and Communications Technology

Tsugumichi Shibata, Shin'ichiro Mutoh, and Atsushi Murase

Abstract

The recent growth in popularity of fiber-to-the-home (FTTH) services and mobile smartphones is resulting in an explosive increase in the volume of communications traffic, and this has led to a subsequent increase in the power consumed by network devices and terminals. In the Feature Articles in this issue, we give an overview of power-reducing and power-saving techniques to implement green information and communications technology, and we introduce technological developments NTT is working on that are designed to reduce the power consumption of network equipment.

1. Introduction

In Japan, the simultaneous proliferation of optical fiber-to–the-home (FTTH) services such as B FLET's and high-speed mobile communications services such as Xi (pronounced *crossy*) has led to widespread daily use of the "anywhere, anytime" Internet access. Many users are now reaping the benefits of leading-edge broadband networks, anticipating the expansion of new application services and innovative terminal devices, and looking forward to further improvements in information and communications technology (ICT) that give them a higher quality of life (QoL). Against this background, the volume of communications traffic centered on image- and video-related services is growing explosively, and it is therefore important to find ways of ensuring that the power consumed by related equipment does not increase. We believe that power reduction is an important research and development challenge in the drive for continuous development of network services that support the creation of an affluent society.

2. Ongoing research and development in Microsystem Integration Laboratories

In November, 2010, the NTT Group drew up a new environmental vision called THE GREEN VISION 2020 [1] for intended application through 2020. We are continuing with our initiatives and research and development (R&D) with the aim of forming a recycling-oriented society by implementing *Green of ICT* and applying *Green by ICT* [1]. In our R&D on circuits and devices for communications at NTT Microsystem Integration Laboratories, we are developing technology that not only prevents any increases in power consumption but also reduces power consumption while simultaneously improving device functionality and performance. We are also conducting innovative research with the aim of achieving extreme power saving systems.

An optical IP (Internet protocol) network is divided into three segments: a core network that covers a wide area, access networks that extend from the core, and network appliances that are connected to the access networks (**Fig. 1**). Of these segments, the access networks consume the largest proportion of power [2], and methods to save power in the access networks are being investigated. R&D is underway on media

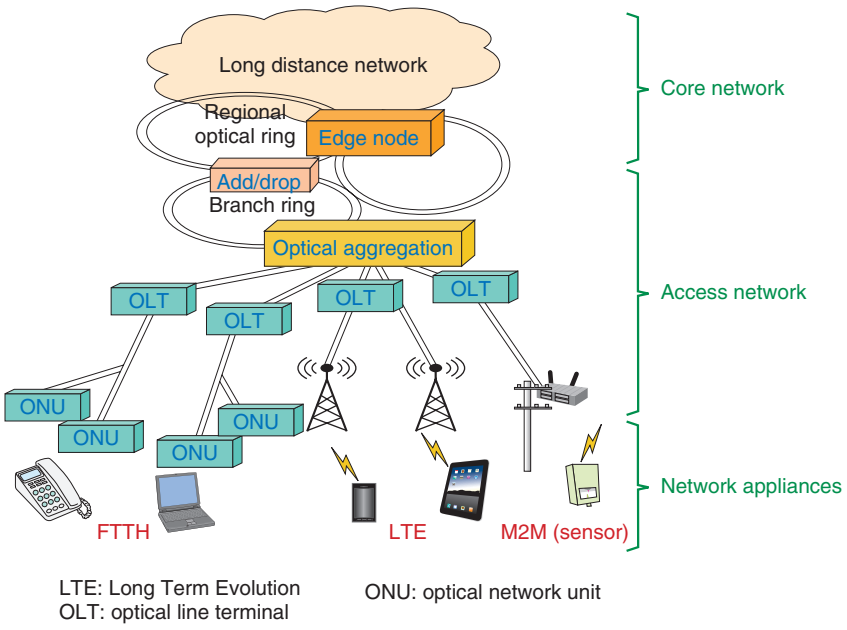


Fig. 1. Conceptual view of IP optical network.

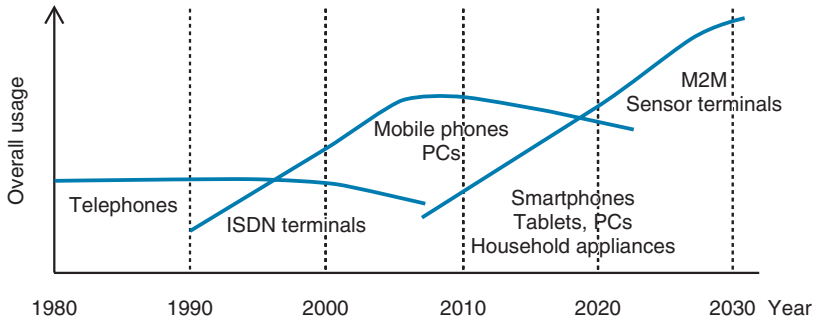
access control (MAC) large-scale integrated circuits (LSIs) for the 10-Gbit/s Ethernet passive optical network (10G-EPON) systems that will be the next upgrade of the FTTH service. Our objective in this research is to achieve reduced power consumption through innovations in circuit architecture and reductions in circuit scale. We are also implementing sleep control functions for optical network units (ONUs) that are expected to have a substantial effect on power saving, and are conducting experiments in order to evaluate the effectiveness of these techniques. On the user side, a trend toward a reduction in the normal usage frequency (operating time) of devices has been observed, so there is much leeway in saving electrical power when devices are not in use.

In core networks, traffic from the access networks is aggregated, and devices such as core routers are required to efficiently accommodate functions for processing large volumes of data in compact equipment. In this case, efforts to reduce power benefit the environment and energy resources and also alleviate design margins relating to heat generation of communications installations. This technology is expected to help reduce installation space requirements, capital expenditure (CAPEX), and operating expenses (OPEX) by enabling high-density installation.

With network appliances, the focus is on reducing power in mobile and sensor terminals. Power-saving technology is directly related to the extension of battery life and will help to improve user-friendliness and reduce maintenance work. The transition in the types of network appliances used over the years is shown in **Fig. 2**. We predict that a huge variety of sensor terminals in the machine-to-machine (M2M) communications form will be widely distributed in the future. Consequently, we are carrying out R&D on ways to achieve much higher levels of power saving in terminal architecture and configuration technology, as well as R&D on energy harvesting technology.

3. LSI power-reduction technology and directions of R&D

Here, we review techniques to reduce power consumption through the appropriate design of large-scale integrated circuits (LSIs), which form the heart of signal processing and communications protocol control equipment. In terms of device technology, we could use compound semiconductor technology or SiGe bipolar complementary metal oxide semiconductor (Bi-CMOS) technology for communication LSIs in the transmitters and receivers of transceivers to improve speed. If we were to focus on power instead, we could use silicon CMOS technology to implement large-scale circuits that provide advanced



ISDN: integrated services digital network
PC: personal computer

Fig. 2. Changing trends in use of network appliances.

digital signal processing or communications protocol control. We review the power consumed by CMOS circuitry below.

The power consumed by a CMOS digital circuit can generally be written as:

$$P = C\,V_{DD}^2\,f + P_{Leak} + P_{I/O}$$

The first term on the right side represents the electrical power consumed through repeated charging and discharging that occurs with the operation of the logic circuitry. The second term is the power dissipation due to leakage current, which has increased as transistors have become smaller and which will dissipate power through leakage despite our best efforts to prevent it. The third term is a characteristic feature of large-capacity signal processing LSIs, which have explicitly added the power consumption of the peripheral input/output (I/O) circuit parts for moving large volumes of data into and out of LSI chips. These parts are formed by various circuits such as those that perform the serial-parallel conversion and timing control of I/O signals and the analog circuits that drive external loads. The power consumption reaches particularly high values in LSIs that input and output large quantities of frames or packets when processing large volumes of signals. This is a continuing major issue in implementing larger throughputs and higher integration levels.

In the first term of the equation, C is the load capacitance of the logic gates (basic circuitry). This also depends on the layout of the wiring, but as a rule of thumb, the value is determined once the generation (nodes) of the fabrication process has been determined. The value V_{DD} is the power voltage, which has dropped from 5 V to 3.3 V as processes have become finer, leading to a corresponding decrease in power consumption. When the latest processes are used, the internal digital circuits are designed to run with a power voltage on the order of 1 V. In addition, f is the actual operating speed (frequency) of the circuitry. If we focus on f, it is clear that the first term can be reduced by lowering f, if it is acceptable for circuit operations to become sluggish or even stop temporarily, depending on the communications situation. This situation is shown schematically by the red line in **Fig. 3**. Control of f can be achieved by clock gating that stops the clock that is distributed to the circuitry, either temporarily or partially.

The power dissipation caused by leakage current (second term of equation) cannot be reduced by clock gating but must be reduced by cutting the power supply. Shutting off power either temporarily or partially is known as power gating. Circuit technology that uses power gating is referred to as multithreshold voltage CMOS (MTCMOS) technology and is well known as an NTT innovation [4].

Skillful use of power gating makes it possible to supply power to necessary functions only when needed, and to let the device sleep when it is not required. This is shown schematically by the green and blue lines in Fig. 3. It may also be possible to implement even finer-tuned power saving by re-examining communications control or by exerting control over the state of traffic that should be processed. The power-saving technique linked to this communications control (**Fig. 4**) is one of the technological development trends in power reduction based on circuit technology for communication LSIs.

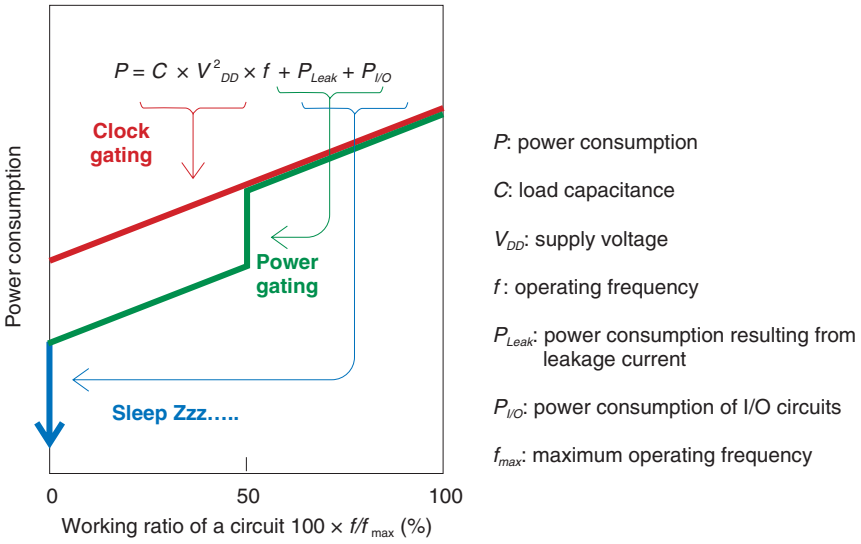


Fig. 3. Power consumption of CMOS LSIs for networks.

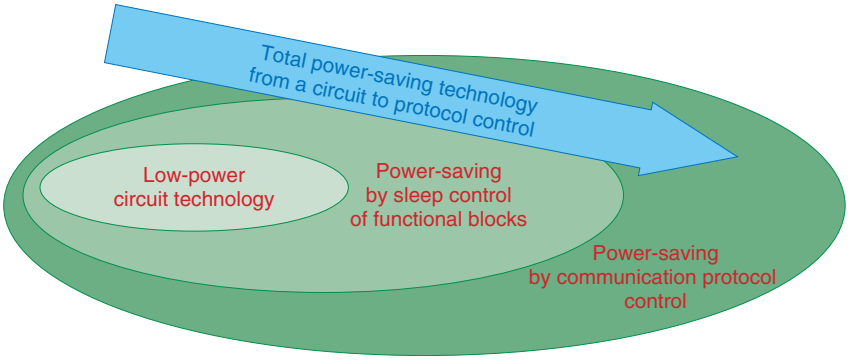


Fig. 4. Direction of our R&D on low-power-consumption equipment.

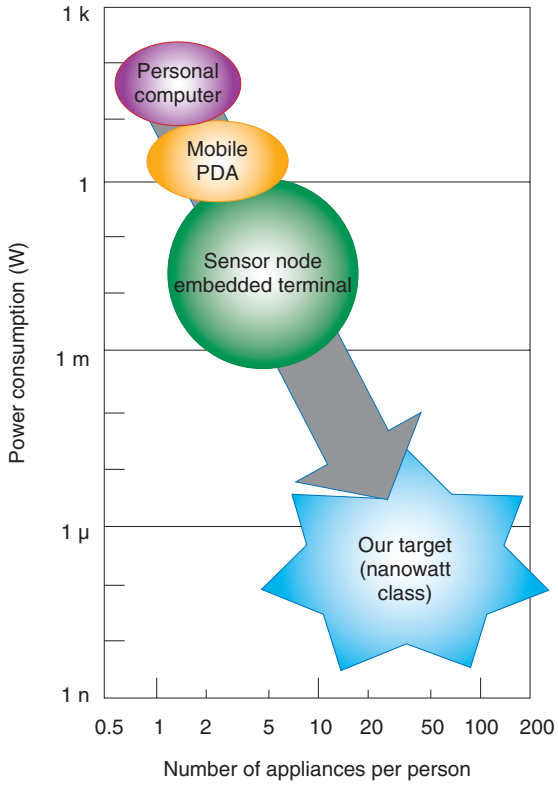
4. Topics and structure of feature articles

The other Feature Articles in this issue introduce six topics we are working on at NTT Microsystem Integration Laboratories.

The second article, "Low-power LSI Techniques for Next-generation FTTH System" gives a detailed description of power reduction technology for control LSIs for the 10G-EPON system [5]. It introduces our efforts to reduce power by scaling down signal processing and communications control circuits. It also introduces the possibility of power-saving in the analog circuits that drive lasers according to the data traffic situation, by burst signal processing technology, which is our technological strength.

The third article, "Energy-saving Technique for High-speed Packet Forwarding LSI" describes a power gating technique for achieving both high throughput and energy-saving performance of a 100-Gbit/s-class high-end router packet-forwarding circuit [6]. The technique uses two parallel forwarding engines that are fully activated when the traffic is heavy and partially powered down depending on the traffic conditions.

The next three articles deal with topics relating to M2M sensor terminals. "Nanowatt Circuit Technology for an Ultrasmall Wireless Sensor Node with Energy Harvester" introduces details of investigations targeted at extremely low-powered sensor terminals [7]. The goal is to develop sensor terminals



PDA: personal digital assistant

Fig. 5. Power consumption target for sensor terminals.

that are able to gather electrical power from the surrounding environmental energy, enabling them to operate autonomously and perpetually. This article also proposes sensing circuits and wireless transmission circuits operating on the order of nanowatts. (**Fig. 5**)

The article entitled "Low Power Consumption Sensor Interface Terminal for Various Telemetry Applications" describes terminal configuration technology that can be applied to existing services and that can accommodate a variety of sensors [8]. Devices for telemetry must be able to operate under battery power for five to ten years without maintenance. It is therefore a technological challenge to determine how they will best be able to respond to such conditions.

The article "Vibrational Energy Harvesting with Microelectromechanical System Technology" introduces attempts to harvest electrical power from vibration energy that is all around us and provides details relating to research into circuits that operate on electrical power on the order of nanowatts [9]. We report on details and the current situation of vibration power-generating technology used in microelectromechanical systems (MEMS) technology.

Finally, in "Integrated Silicon-based Optical Interconnect for Fast, Compact, Energy-efficient Electronic Circuit Systems" [10], we introduce the state of R&D into silicon photonics technology that will be used to convert the input-output interfaces of devices that handle large volumes of signals to fiber optics, reduce the previously described power consumption term $P_{I/O}$, and also attempt to help make devices even more compact and highly integrated by integrating and combining optical and electrical processing.

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Tsugumichi Shibata
Executive Manager, Ubiquitous Interface Laboratory, NTT Microsystem Integration Laboratories.

He graduated from Tokyo National College of Technology in 1980 and received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Tokyo in 1983, 1985, and 1995, respectively. In 1985, he joined NTT, where he has been engaged in research on electromagnetic-field analyses and the design of high-speed optical front-end ICs and protocol-control LSIs for data transmission systems. From 1996 to 1997, he was a Visiting Scholar at the University of California at Los Angeles (UCLA), where he did research on diakoptics in numerical simulations. He served as a vice president of the Institute of Electronics, Information and Communication Engineers (IEICE) Electronics Society from 2007 to 2009, an Executive Committee member of the VLSI Symposia from 2007 to 2012 and of the Asia-Pacific Microwave Conference (APMC) in 2006 and 2010. He is a senior member of IEEE and IEICE and is the chair of the Electronics Simulation Technical Group of IEICE.

Shin'ichiro Mutoh
Project Manager, First Promotion Project, NTT Microsystem Integration Laboratories.

He received the B.E. and M.E. degrees in electronic engineering from Chiba University in 1986 and 1988, respectively. In 1988, he joined NTT, where he was initially engaged in research on ultrahigh-speed BiCMOS SRAM and low-power CMOS SRAM circuits. He was also involved in R&D of low-power and low-voltage digital circuit technologies, especially multiple-threshold-voltage CMOS (MTCMOS) circuits. His current interests are ultralow-power wireless sensor node architecture and circuit design for advanced sensor network systems and LSI design for optical telecommunication networks. He served as a Program Committee Member of the Symposium on VLSI Circuits from 2008 to 2011. He is a member of the International Solid-Sate Circuits Conference (ISSCC) 2013 Technology Direction Subcommittee and of the Japan Society of Applied Physics (JSAP) Executive Committee of Symposia on VLSI Technology and Circuits.

Atsushi Murase
Director, NTT Microsystem Integration Laboratories.

He received the B.E. degree in electronics and communications engineering and the Ph.D. degree from Waseda University, Tokyo, in 1981 and 1991, respectively. He has broad experience in 1G to 3G mobile communication systems development especially involving base stations, controllers, and 3G FOMA terminals that he attained through more than 25 years spent on mobile communication R&D at NTT and NTT DOCOMO. He worked at British Telecom Labs in UK from 1989 to 1990 as part of a researcher exchange. He was President & CEO of DOCOMO Communications Laboratories Europe GmbH in Munich, Germany from 2002 to 2005. He also served as Managing Director of Research Laboratories, NTT DOCOMO from April 2007 to June 2012.

Low-power LSI Techniques for Next-generation FTTH System

Mamoru Nakanishi, Hiroshi Koizumi, Sadayuki Yasuda, Tomoaki Kawamura, Shoko Ohteru, Naoki Miura, and Minoru Togashi

Abstract

Demand for reduced power consumption of network devices is growing as Internet protocol traffic increases and fiber-to-the-home service penetration expands. This article describes our low-power-consumption technology developed for application to medium access control large-scale integrated circuits (LSIs) and analog front-end integrated circuits. Power saving is achieved with dynamic control according to the traffic state or link state, which reduces power consumption in LSIs and in entire network systems.

1. Introduction

The number of fiber-to-the-home (FTTH) subscribers in Japan has reached more than 20 million, and the volume of downstream traffic is now as high as 1.7 Tbit/s [1]. The Gigabit Ethernet passive optical network (GE-PON) is widely used as the main access network. The expansion of cloud computing applications, 3D (three dimensional) video, and high-definition video (4K video) will likely lead to further increases in Internet traffic.

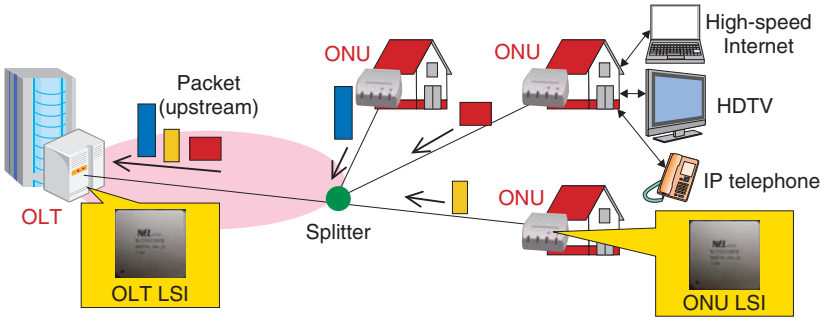
The deployment of 10G-EPON, which is ten times faster than GE-PON, is expected in order to handle the increasing volume of traffic. The international standard for the 10G-EPON physical link layer (IEEE 802.3av) [2] was established in 2009. System-level 10G-EPON standards (IEEE 1904.1 SIEPON) are now being studied, with completion aimed for in 2013.

An overview of the 10G-EPON system is shown in **Fig. 1**. An optical line terminal (OLT) is located at a central office, and several optical network units (ONUs) are installed at each user premises. The ONUs share the optical fiber connected to the OLT through a splitter. The OLT must support 10G and 1G dual-rate communications to accommodate the coexistence of three different types of ONUs: symmetric 10G ONUs, asymmetric 10G ONUs, and 1G ONUs.

Reducing the power consumption of access network systems is a pressing issue. ONU power consumption accounts for 60% of power consumed by the entire network, including the Internet protocol (IP) core network, because the number of ONUs is proportional to the number of subscribers. The power consumption of access networks accounts for more than 80% of the total network power consumption, including the OLT and aggregation network switches.

In the 10G-EPON system, the need for dual-rate burst lG/10G reception will lead to an increase in hardware scale and power consumption. Nevertheless, the dual-rate reception is necessary in order to accommodate the existing GE-PON, which will allow the coexistence of 10G and 1G data paths, and to accommodate multiple forward error correction (FEC) and encryption methods for 10G and 1G data communications. The following techniques for reducing the power consumption of a practical 10G-EPON system are therefore very important.

- Reducing the number of transistors and the power consumption of LSI devices
- Downsizing and reducing the power of the system by incorporating peripheral components into large-scale integrated circuits (LSIs)



HDTV: high-definition television
IP: Internet protocol

Fig. 1. Overview of the 10G-EPON system.

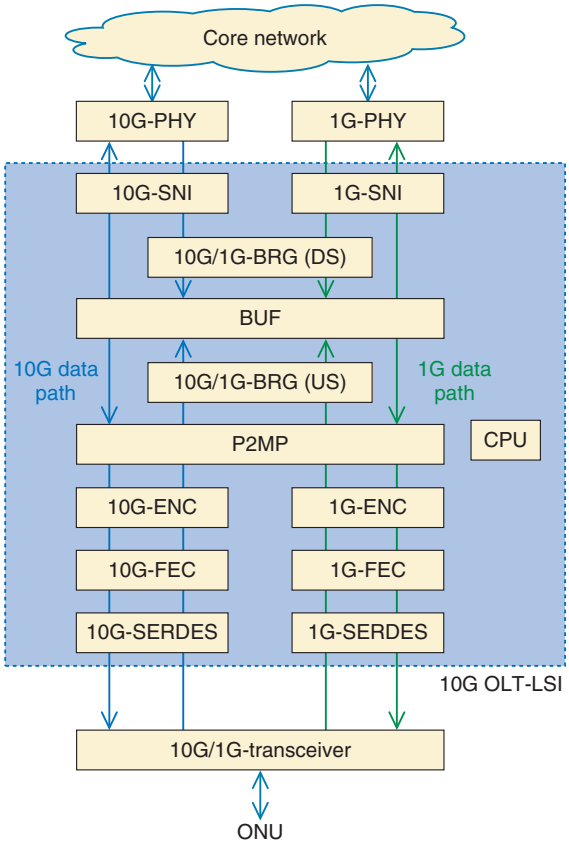


Fig. 2. 10G-EPON MAC-LSI (OLT).

- Controlling the power consumption of devices according to the traffic and operating status

2. 10G-EPON medium access control (MAC) LSI

2.1 Architecture

We have developed a chipset for the dual-rate 10G/1G EPON OLT MAC control LSI and the symmetric/asymmetric supporting 10G-EPON ONU MAC control LSI, which integrates all functions specified in the IEEE 802.3av standard in 40-nm complementary metal oxide semiconductor (CMOS) technology for the first time. A block diagram of the dual-rate 10G/1G EPON OLT is shown in **Fig. 2**.

The OLT LSI can independently transmit 10- and 1-Gbit/s frames through two system network interfaces (SNIs) for 10 and 1 Gbit/s data rates with a core network. In this OLT LSI, 10-Gbit/s frames are deserialized to a 64-bit width at 156 MHz, and 1-Gbit/s frames are deserialized to an 8-bit width at 125 MHz. Then both the 10G and 1G frames are transferred to the bridge block (BRG). In the BRG and buffer block (BUF), 10G and 1G data paths are multiplexed, and frame operations such as priority control and destination search are performed. The point-to-multipoint link control block (P2MP) manages and controls the link status of the connected ONUs and grants permission for upstream transmission to the ONUs. The P2MP also controls the frame reception timing of burst upstream signals, so it is considered to be the heart of the LSI. Thereafter, the LSI is connected to a 10G/1G dual-rate transceiver through the encryption block (ENC), forward error correction block (FEC), and serializer-deserializer block (SERDES), which converts the multiplicity of input/output signals.

The 1G and 10G data paths are separated at the FEC and ENC blocks because the standard

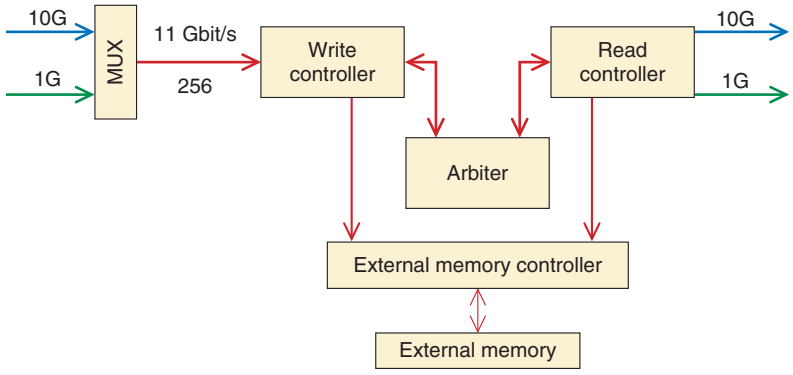


Fig. 3. Block diagram of the buffer control block.

specifications for FEC and encryption are different for 1G and 10G. In contrast, the data paths for 1G and 10G are shared at the BRG and BUF blocks in order to reduce the size of the BRG and BUF circuits.

2.2 Downsizing of encryption circuit

To distinguish and receive 1G burst signals from asymmetric 10G-ONUs and conventional 1G-ONUs, an encryption method must be selected, and decryption must be properly performed. If we employ a method that distinguishes the decryption algorithms by examining the received frame, the OLT has to buffer the frame during the time it takes to examine it and dynamically select the algorithm. This requires an additional frame buffer and increases the OLT latency.

The OLT already knows the upstream receive time slot and the type of source ONU because the OLT assigns the bandwidth for ONUs so that upstream frames from each one do not overlap each other. The decryption controller we implemented can evaluate decryption methods and set up the decryption algorithm before the frames are received.

The dynamic bandwidth allocation information-based scheduling method eliminates the need for additional upstream-frame buffering and makes it possible to change the decryption algorithm burst by burst. Not only can significant hardware overhead be avoided but also the increase in latency can be suppressed.

2.3 High-throughput data-path construction

The details of the BUF block are depicted in **Fig. 3**. A 10-Gbit/s data path and a 1-Gbit/s data path are multiplexed in the multiplexer (MUX) to a 256-bit width. This is because throughput greater than 22-Gbit/s for the read and write operations of memory access is necessary for full wire-rate transmission. In addition, to prevent throughput degradation by continuously writing short frames such as 64-byte frames to memory, a memory write controller writes frames to external memories only when more than 1 kbyte of frame data is stored in the buffer memory in the write controller. Frames of both 10G and 1G data are first stored in the same buffer memory and then sent from the buffer in the order of priority determined by the BRG block. In this way, we reduce the number of external memories and the size of the circuits, and we suppress the delay.

2.4 Flexible functionality

The OLT P2MP manages the states of ONUs such as the link state and power-saving state. The OLT or ONU transmits and receives the control frame to and from each other and changes their state. To prevent signals from the ONUs colliding in the upstream, the OLT distributes the timing in 16-ns clock order to all ONUs for synchronization. The main functions of the P2MP are as follows:

- Carrying out multiplexing and demultiplexing in order to send and receive data frames and control frames.
- Generating local reference time and controlling signals for each block in the LSI
- Managing the ONUs, including link-status monitoring, control-frame generation and transmission, and control-frame reception and parsing.

To allow the 10G-EPON systems to be adapted to various services such as triple play or bandwidth-guarantee, the P2MP block should be able to perform protocol processing between the ONU and OLT with

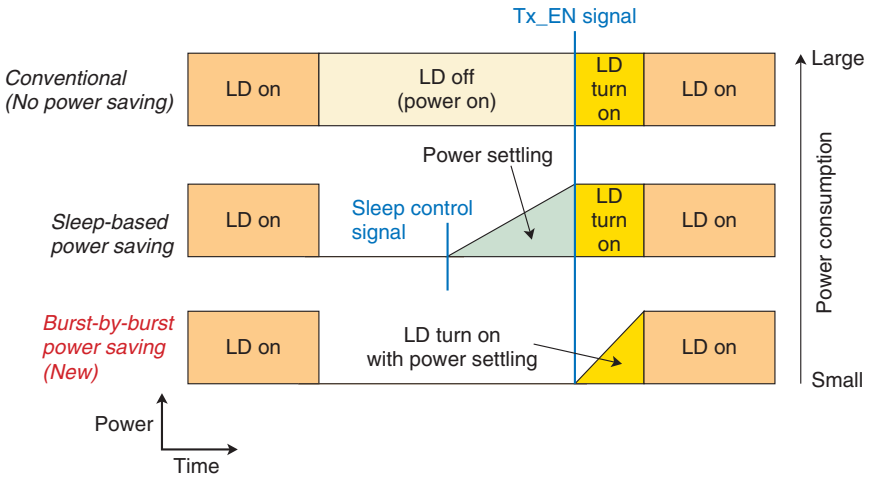


Fig. 4. Concept of the proposed burst-by-burst power saving.

extendibility and flexibility. Moreover, flexible protocol processing can support effective ONU sleep management to save power. Software-hardware cooperation in protocol processing is an efficient way to achieve extendibility and flexibility. The function which needs precise control for maintaining the timing accuracy and throughput requirements was extracted as a hardware execution function. By contrast, flexible ONU management is assigned to software. This assignment enables the P2MP to modify the management of each ONU state and transmit control frames with any format. Thus, the OLT with traffic control and link status monitoring implemented in software enables us to achieve ONU sleep management for power saving.

3. Burst-mode laser diode driver (BLDD)

3.1 Power consumption of burst-mode transmitter

Reducing power consumption is a pressing need for the burst-mode transmitter because 10–20% of the ONU power is consumed by the BLDD. A simple approach for power saving is to shut down the transmitter when there are no upstream optical bursts. However, this approach can be applied only during long periods of no data transmission because of the long settling time [3]. When a PON system has 32 branches, the maximum number allowed by IEEE 802.3av, each laser diode (LD) can be turned off for 97% (= 31/32) of the time on average. The conventional BLDD consumes power continuously irrespective of the existence of traffic. The sleep-based power saving requires a settling time to power up, and a sleep control signal is required in addition to the transmit enable (Tx_EN) signal currently used as the standard. The transmitter receives the Tx_EN signal from the PON control IC and turns on the LD after power is recovered. In our burst-by-burst power saving scheme, both the power and LD turn on simultaneously when the Tx_EN signal is received (**Fig. 4**). Our proposed BLDD can exploit the short absence of transmission data by shortening the power settling time to approximately 3% of the maximum LD turn-on delay of 512 ns defined in IEEE 802.3av, thereby saving power efficiently.

3.2 BLDD with power-saving feature

A block diagram of the proposed BLDD circuit and a photograph of a test chip that was designed and fabricated in 0.18-μm SiGe BiCMOS (bipolar CMOS) technology are shown in **Fig. 5**. To quickly restore power from the power-saving mode, a current switch is added to the current source of each block. The gate circuit is put in the front stage of the output driver to keep the input signal at the differential low level when the laser is off with power saving. Maintaining the input at a low level makes the laser extinction more reliable. The gate circuit has to act as a pre-buffer for the large output driver and therefore consumes a relatively large current when the laser is on. However, because the low-level output does not need a large bandwidth, we are able to implement a mechanism in the gate circuit that allows the circuit

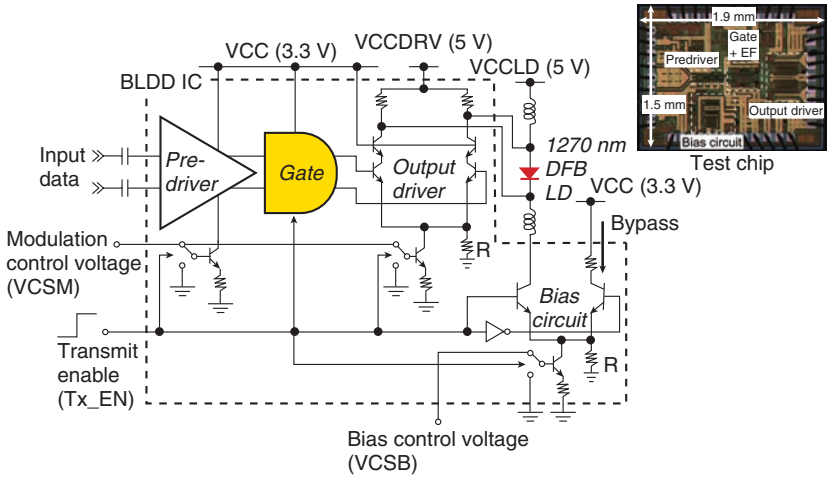


Fig. 5. Block diagram of the proposed BLDD circuit and photo of the test chip.

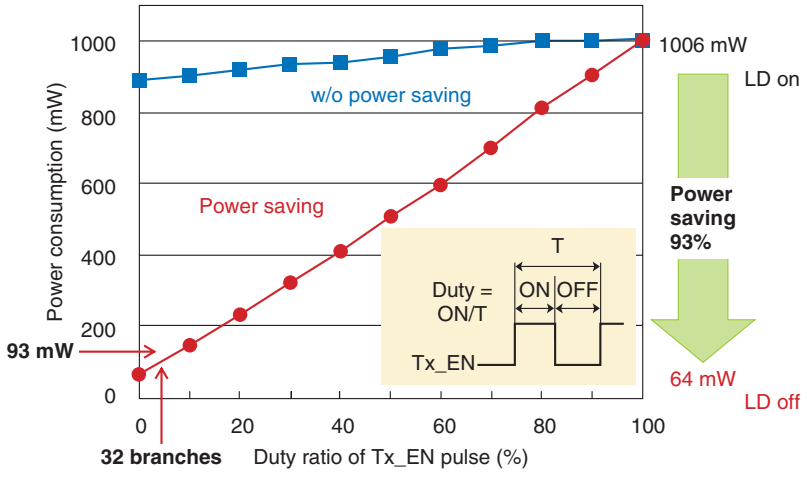


Fig. 6. Measured power consumption of BLDD.

to reduce power consumption itself during the LD-off state. The combination of burst control mechanisms and current switching enables both effective power saving and complete extinction of the laser [4], [5]. The distinctive feature is that both the burst operation and power saving are controlled by only a single Tx_EN signal.

The input data stream for all measurements was a 2^{31}-1 PRBS (pseudo-random bit sequence) NRZ (non-return-to-zero) signal with a data rate of 10.3125 Gbit/s. The measured power consumption for burst-by-burst power saving operation and conventional non-power-saving burst operation with various duty ratios of Tx_EN signal pulsing are shown in **Fig. 6**. The Tx_EN pulse frequency was 2 MHz. The power consumption is dramatically reduced from 1006 to 64 mW when the laser is turned off with the power-saving operation. In contrast, the change in power consumption for the conventional burst operation is very small. Our BLDD reduces power consumption by more than 90% when the PON system has 32 branches.

The transient optical waveforms after fourth-order Bessel-Thomson filtering with the burst-by-burst

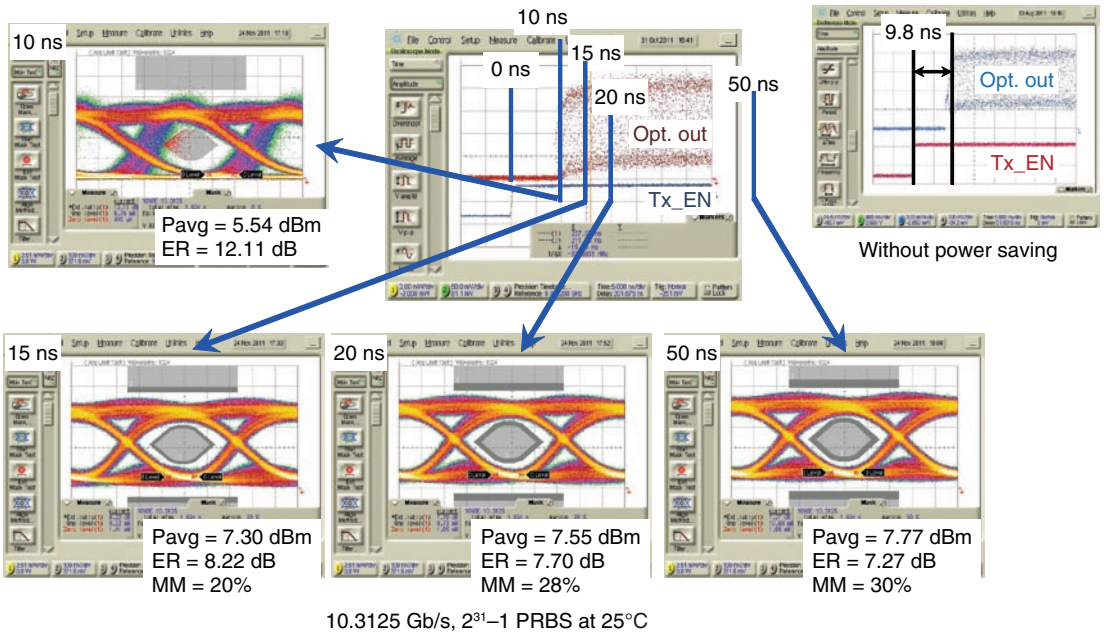


Fig. 7. Transient optical waveforms with the burst-by-burst power-saving operation.

power saving operation are shown in **Fig. 7**. The waveforms were measured 10, 15, 20, and 50 ns after the transmission was enabled. The BLDD demonstrates a sufficient average optical launch power of 7.3 dBm, an extinction ratio of 8.22 dB, and a mask margin of 20% at 15 ns. The mask margin increases to 30% at 50 ns. These results show that our BLDD quickly recovers from the power-saving mode in 15 ns or less, which is 34 times faster than the turn-on time defined in IEEE 802.3av PR30 standards. Without power saving, the turn-on time is 9.8 ns, which means the penalty for the power saving is under 6 ns. This is the first burst-by-burst power saving circuit that satisfies the IEEE standard with a sufficient margin.

4. Conclusion

We introduced techniques for designing MAC LSIs and burst-mode laser driver ICs to achieve power saving in the 10G-EPON system.

The increase in communications traffic is expected to continue, which will inevitably result in equipment becoming larger. To control power saving of an entire system, electric power control for power saving at the LSI level and cooperative operation between many connected LSIs and ICs are needed.

We will work on implementing a control mechanism for LSIs to achieve such system-level power saving.

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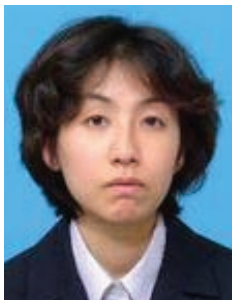

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Energy-saving Technique for High-speed Packet Forwarding LSIs

Sadayuki Yasuda, Shoko Ohteru, Yasuyuki Itoh, Koji Yamazaki, and Masami Urano

Abstract

Network traffic is increasing exponentially, and this requires packet forwarding circuits with higher capacity, which strengthens the demand for higher energy efficiency in these circuits. This article describes an energy-saving technique for high-speed packet forwarding circuits.

1. Introduction

The packet forwarding circuit in a communication network delivers data from the sender to the recipient. This circuit looks up the media access control (MAC) address (layer 2 switch) and IP (Internet protocol) address (layer 3 switch) that are contained in the inbound packet header and performs a routing function in which it sends the packets to the output ports. NTT Microsystem Integration Laboratories has been carrying out research and development (R&D) on circuit configurations for implementing a next-generation packet forwarding large-scale integrated circuit (LSI). Our research includes high-speed circuit technology for achieving 100-Gbit/s-class packet-forwarding speeds, reduced power consumption, higher performance with the same or lower power consumption, and functional expansion by enabling cooperation between a forwarding LSI and a programmable LSI to allow flexibility in adding future services. Here, we explain our energy-saving technique.

2. Increase in forwarding performance and energy efficiency

Research efforts are intensifying to achieve faster processing speeds in network devices so they will be able to process the continually increasing amounts of traffic. The forwarding speed at the wavelength of the trunk network is over 100 Gbit/s (**Fig. 1**) [1]–[3], and the forwarding speed of Ethernet from Datacom Systems is not far behind. The forwarding circuits that route such high-speed packets at the line rate must process a large volume of packets in a very short time. Therefore, either the circuits that implement that function must be operated at a high clock frequency, or the processing must be done by multiple circuits in parallel. Development to suppress the increase in power consumption that comes with these processes is an increasingly important issue from the viewpoint of energy conservation.

3. Energy-saving methods

The main approaches to saving energy in LSIs are shown in **Fig. 2**. These are frequency scaling, in which the frequency of the clock that drives the circuit is lowered, clock gating, in which the clock is periodically stopped, and power gating, in which the power is turned off [4]. The basic principles of these methods when they are applied to packet forwarding can be illustrated through the example of package sorting and delivery. In normal operation, the addresses are sorted and the packages are delivered at high speed. When there are few packages to be delivered, the delivery speed is reduced. When there are no packages to be delivered, the sorting process is put on stand-by, from which it can begin again at any time, and delivery is stopped. The last method is equivalent to stopping both sorting and delivery. In other words, the clock frequency (f) is set to the maximum (f_{max}) during normal operation to obtain the full performance of the circuit, and the circuit is run on the

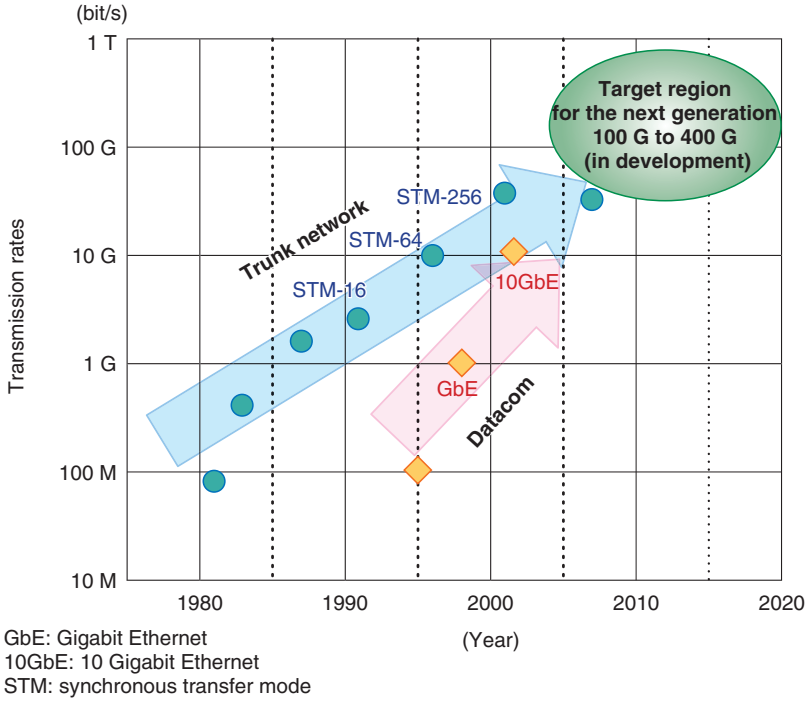

Fig. 1. Next-generation communication transmission rates.

	Energy-saving method	Forwarding Delivery speed Sorting	Clock frequency control	Forwarding circuit power supply (V_{DD})	Time needed to restart operation	Energy-saving effect
(1)	(Normal operation)	On Forwarding process / Fast sending	$f=f_{max}$	On	–	–
(2)	Frequency scaling	On / Slow sending	$0<f<f_{max}$	On	–	△
(3)	Clock gating	On (stand-by) / Stop	$f=0$: Off	On	○	△
(4)	Power gating	Off / Stop	–	Off (V_{DD}=0)	△	○

Fig. 2. Basic principles and effects of energy-saving methods.

prescribed power supply (V_{DD}). Frequency scaling conserves energy by reducing the clock frequency (f) according to the amount of processing. As the frequency is lowered, the energy-saving effect increases. Both clock gating and power gating are applied when the amount of processing drops to zero. Clock gating reduces power consumption by stopping the clock signal from being provided to the circuit. Because only the clock is stopped, the circuit remains in stand-by mode, so circuit operation can begin immediately when the clock signal is restored. For that reason, clock gating can be applied for very short time periods, such as in the time interval between packets. However, the power supply (V_{DD}) remains on, so it is

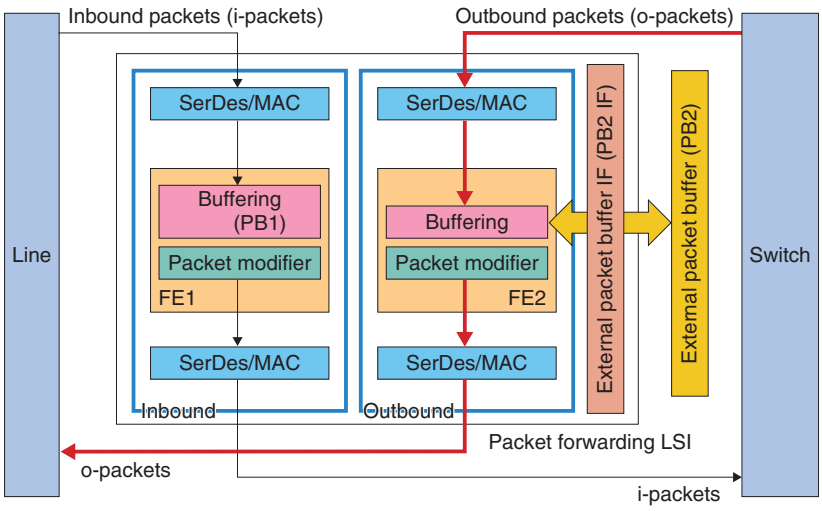

Fig. 3. Basic configuration of packet forwarding circuit.

not possible to prevent power consumption caused by leakage current, and consequently, the energy-saving effect is not that large. Power gating temporarily or partially stops the power supply. Because power gating can prevent power consumption due to leakage current, it is the most effective of the energy-saving methods. However, once the power is turned off, some time is required to restore it, so this method is applied to circuits that operate for a certain period of time and then stop.

4. Requirements and issues

When packets are inbound at 100-Gbit/s-class data rates, the interval between packets is measured in units of nanoseconds (10^{-9} seconds), so the forwarding circuit must operate constantly. Even when no packets are inbound, the circuit must always remain in a stand-by state that allows immediate forwarding at high throughput when packets arrive without notice. This requirement has made it difficult to apply power gating, which has a recovery time measured in microseconds (10^{-6} seconds). We therefore developed an energy-saving technique in which power gating is applied by concentrating packets in a packet processing block when throughput is low. We explain that technique in detail below.

5. Power gating technique

The basic configuration of a packet forwarding LSI is illustrated in **Fig. 3**. The functional configuration includes processing of both inbound packets coming from the line (i-packets) and outbound packets going to the line (o-packets). Received packets pass through the serial-parallel converter (SerDes) and the media access controller (MAC) and are buffered and processed for transmission. The packets then pass through the MAC and SerDes and are forwarded. This packet processing sequence is similar for i-packets and o-packets, both in content and procedure, so the two forwarding engines (FE1 and FE2) have approximately the same functions. The i-packet data rate can easily be estimated in advance from the network interface input speed and the number of line ports, but the data rate of the o-packet input from the switch (SW) can fluctuate greatly according to the switching by SW. Therefore, an external packet buffer (PB2) and an interface circuit for it (PB2 IF) are provided so that a packet buffer of appropriate capacity according to the location can be implemented to absorb the data rate fluctuation.

A power gating technique for achieving both high throughput and energy-saving performance when packets are input at short intervals and without notice is illustrated in **Fig. 4**. During normal operation, the processing of the inbound and outbound packets is done by the respective FEs. The forwarding throughput of each FE is 100 Gbit/s, so forwarding can be done at a total data rate of 200 Gbit/s. However, when traffic is light, the forwarding can be done by just one of the two FEs, and power consumption can be reduced by switching the packet path so that the packets inbound from the line and the packets outbound to

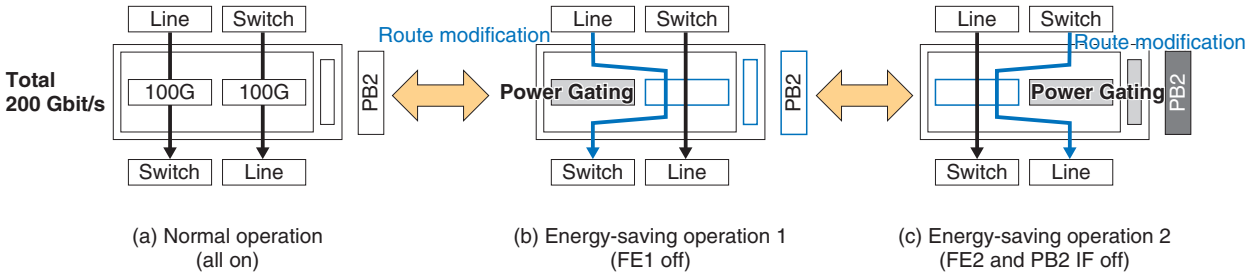

Fig. 4. Power gating technique.

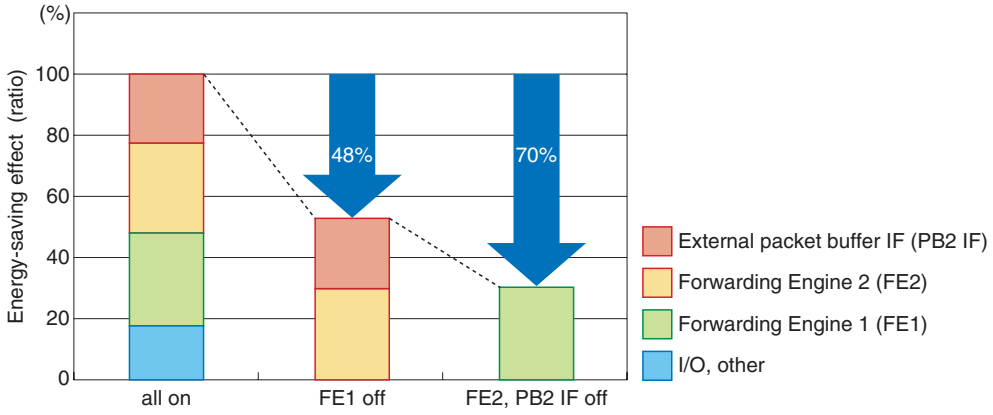

Fig. 5. Energy-saving effect of power gating.

the line are both processed by the FE on the right side. In that case, the power to the FE on the left can be turned off to conserve energy (energy-saving operation 1; FE1 off). Furthermore, when traffic is light and the internal packet buffer is sufficient to absorb fluctuations in the data rate, the packets are funneled to the FE on the left side and all packets are processed by that FE. The power to the FE on the right side and the external packet buffer can be turned off to further reduce power consumption (energy-saving operation 2; FE2, PB2, and packet buffer IF are powered off).

6. Itemized power savings

The energy-saving effect obtained by applying power gating in which the packet path is changed so that all the forwarding is done by one of the FEs and the power to the other FE is turned off are presented in **Fig. 5**. The power-gated functional blocks include forwarding engine 1 (FE1), which is off in energy-saving operation 1, forwarding engine 2 (FE2), and the external packet buffer interface (PB2 IF), which are turned off in energy-saving operation 2, and input-output circuits (I/Os), which are off in both energy-saving operations 1 and 2. The energy savings are 48% for energy-saving operation 1, in which one FE and some I/Os are off, and 70% for energy-saving operation 2, in which PB2 IF is also off.

7. Conclusion

The high-throughput packet forwarding LSI is equipped with many high-speed input-output circuits for receiving and forwarding at high data rates and various MAC processing circuits for flexibly handling a variety of protocols. We intend to expand our energy-saving efforts beyond the results shown in Fig. 5 to include those other constituent elements to achieve even further energy savings.

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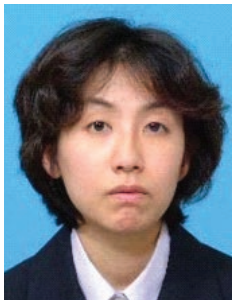

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Nanowatt Circuit Technology for an Ultrasmall Wireless Sensor Node with Energy Harvester

Shoichi Oshima, Kenichi Matsunaga, Toshishige Shimamura, Hiroki Morimura, and Mitsuru Harada

Abstract

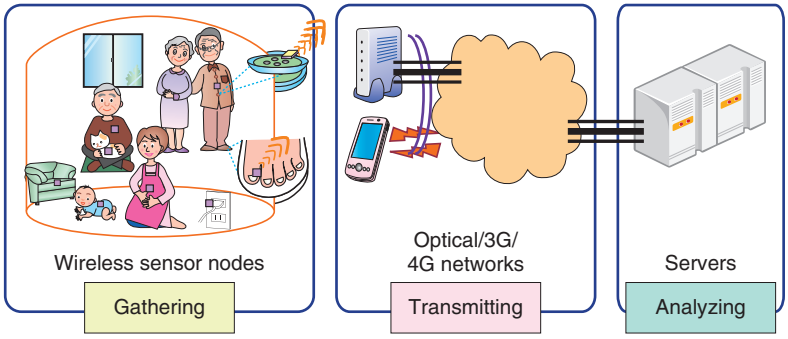
This article describes an ultrasmall wireless sensor node (WSN) that is powered by an energy harvester. The small WSNs can be mounted on any kind of object without increasing their volume, and the energy harvester provides power without having to worry about battery life. However, it is difficult to achieve a WSN that is both ultrasmall and yet still has sufficient power; the smaller the energy harvester is, the less power it generates. We have developed two nanowatt circuit techniques to address this issue. One is a sensing circuit that converts signals with vibration energy. The other is a wireless circuit that uses a quick startup ring oscillator and pulse modulation with an intermittent-driving radio frequency circuit.

1. Introduction

Wireless sensor networks that can gather and analyze trivial information such as vibration, temperature, angles, or positions will lead to the development of new services [1]–[4]. For example, a current sensor attached to electrical appliances in a house can detect how much electricity is used or saved over time, and a sensor that can detect patterns in vibrations caused by wind can indicate cracks in concrete structures. In addition, wireless sensor networks make it possible to provide machine-to-machine (M2M) networks where appliances operate voluntarily without human instructions. An image of a wireless sensor network is shown in **Fig. 1**. The network consists of wireless sensor nodes (WSNs) that can be mounted on any object or living thing to monitor environmental or physical conditions, on master receivers that are connected to the network to collect information from the WSNs, and on servers to store and analyze data.

Our concept is to make the WSNs ultrasmall and to drive them with an energy harvester. The small WSNs can be mounted on any object without increasing the object's volume. The energy harvester draws ambient energy from the surrounding environment. This means that the conventional battery is unnecessary as a power source, and consequently, there are no concerns about battery life. These two aspects also reduce the cost of the WSNs and make them less intrusive, which allows a greater range of applications. Unfortunately, there is a conflict between energy harvesting and node miniaturization; as the energy generator becomes smaller, so does the generated power. In this article, we describe ultralow power, nanowatt circuit technology that we developed to address this problem.

This article is organized as follows. Section 2 describes the energy harvester and nanowatt circuit technology. Section 3 covers the components and circuits of the WSN, and section 4 concludes the article.



3G, 4G: 3rd & 4th generation

Fig. 1. Image of the wireless sensor network.

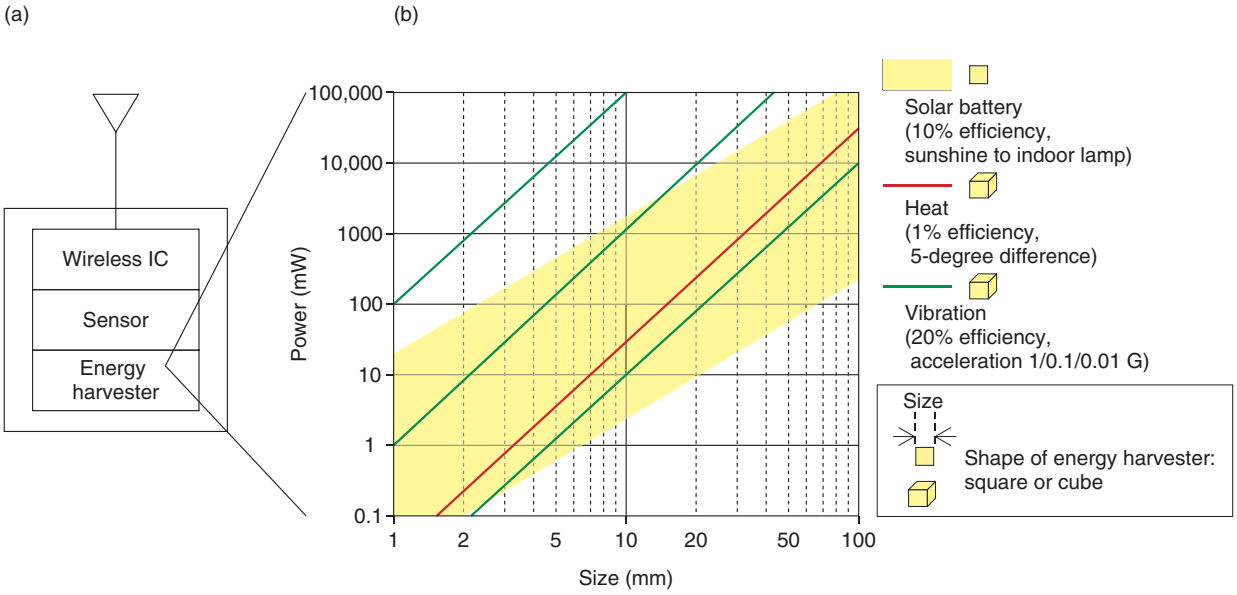


Fig. 2. (a) Minimum WSN configuration and (b) amount of power generated by various sizes of energy harvesters.

2. Nanowatt circuit technology

The minimum configuration of the WSN energy harvester, sensor, and wireless integrated circuit (IC) is shown in **Fig. 2(a)**. We first discuss the energy harvester and then explain the sensing circuit and the wireless configuration.

2.1 Energy harvester

The size of the energy harvester versus the energy generated from ambient heat, vibration, and light sources is shown in **Fig. 2(b)** [5]. The shape of the solar battery is considered as a square, and the others as cubes. Naturally, more energy degradation occurs as the size of the harvester decreases. The energy source that is selected therefore depends on the usage conditions and energy requirements.

For example, there is a good source of heat when WSNs are mounted on human skin or on a large-scale integrated circuit (LSI) of a computer. However, the energy conversion efficiency is low in this case, and a heat waste structure is needed to convert energy.

Vibration is a good energy source for WSNs mounted on humans or vehicles, but space is needed for the vibration generator. Further, the vibration frequency depends on the shape and the material of the generator,

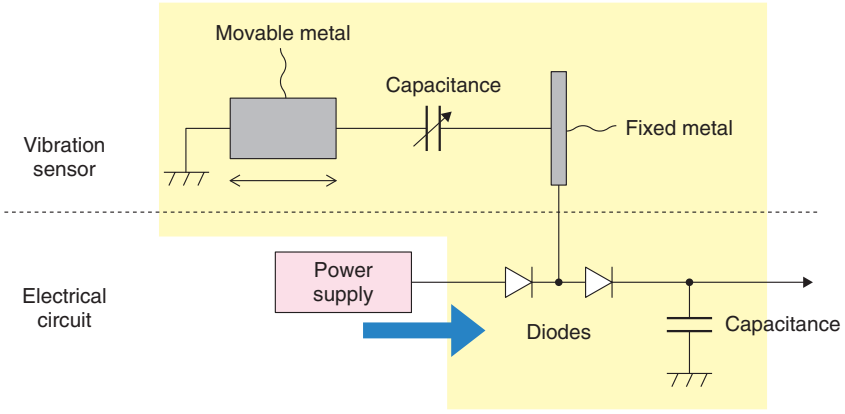


Fig. 3. Vibration conversion circuit with movable metal component.

which limits the flexibility for modeling the generator.

Light is a good energy source only when the light is irradiated. The generated power is affected by the light source, and the intensity of light in different environments, for example, a dark wine cellar, and a sandy beach on a sunny day, can vary dramatically.

Whichever energy source is chosen, the generated power for a WSN less than 1 cm in size under stable conditions, such as when there is no one in a room, is at most 1 μW. To drive all blocks of the WSN with such low energy, nanowatt circuit technology is required.

2.2 Sensing circuit technology [6]

Here we introduce a vibration sensing circuit with nanowatt power consumption. The vibration structure is usually a passive device that consumes little power. However, the conversion of the vibration signal to an electrical signal is the most important point.

The configuration of the vibration sensing circuit is shown in **Fig. 3**. A movable component made of metal forms a capacitor that is connected to the power source. When this component vibrates, its capacitance vibration pattern changes. This results in current being pulled from the power source, which is the same as what happens in a charge pump operation. Thus, the vibration signal is changed into an electrical signal through the use of vibration energy rather than electrical energy, which consumes no electrical power. The measured power consumption of this circuit is only 0.7 nW.

2.3 Wireless IC technology [7]

In this subsection we introduce an ultralow power wireless transmitter that uses intermittent pulse train modulation.

Let us start by first examining a conventional wireless system. The power consumption over time for one-time data transmission is depicted in **Fig. 4(a)**. To transmit data, first, the wireless circuits turn on. However, some startup time is necessary before data can be transmitted. The main operations that make up the startup time are oscillator stabilization and IC reset and initialization. These operations require about 10 ms when the system uses a crystal oscillator to lock the phase-lock loop circuit. The wireless system then starts to transmit the data. During the data transmission, the power consumption consists of the power for driving the circuits and the power transmitted to the air. In theory, only the power transmitted to the air is required for wireless communications. As little power as possible should be used for oscillator stabilization and for driving the circuits.

Our wireless system is shown in **Fig. 4(b)**. We use two key techniques to reduce the total power consumption. One is a quick startup circuit to cut off the energy loss during the stabilization time. The other is the use of a 1-symbol intermittent pulse train instead of a continuous wave, so that when the pulse stops the radio frequency (RF) circuits also stop in order to reduce the energy needed to transmit 1-symbol data.

The total energy for transmitting data is shown in **Fig. 4(c)**. When the length of the transmitting data is long, the 1-symbol energy is dominant in the total energy, and when the data length is short, the stabilization energy is dominant. The proposed system can reduce the energy used for both startup and data transmission and achieve lower energy than a conventional system.

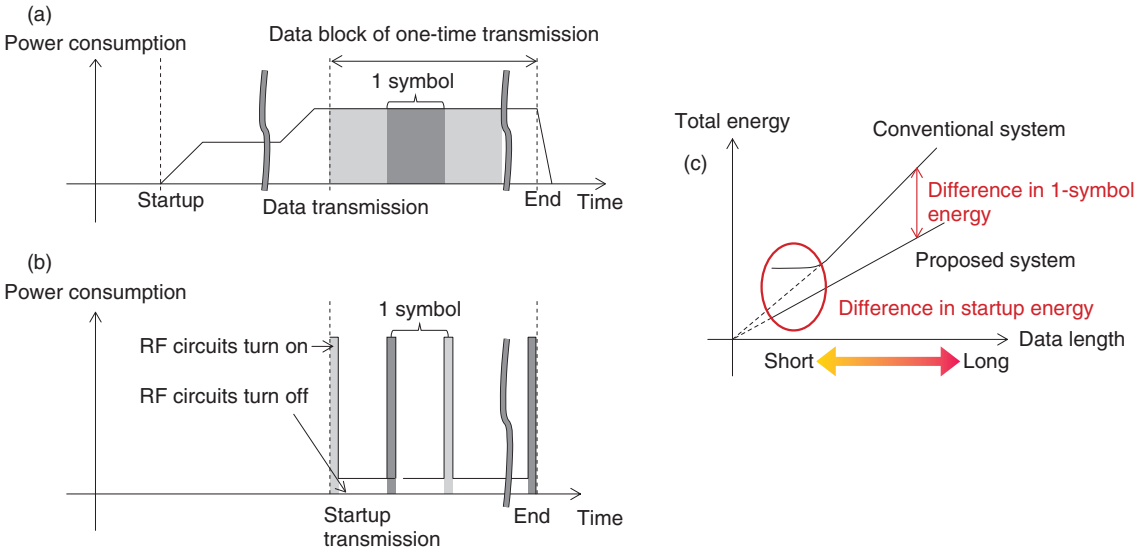


Fig. 4. Power consumed to transmit data from startup to end of data block. (a) Conventional system, (b) proposed system, and (c) total energy.

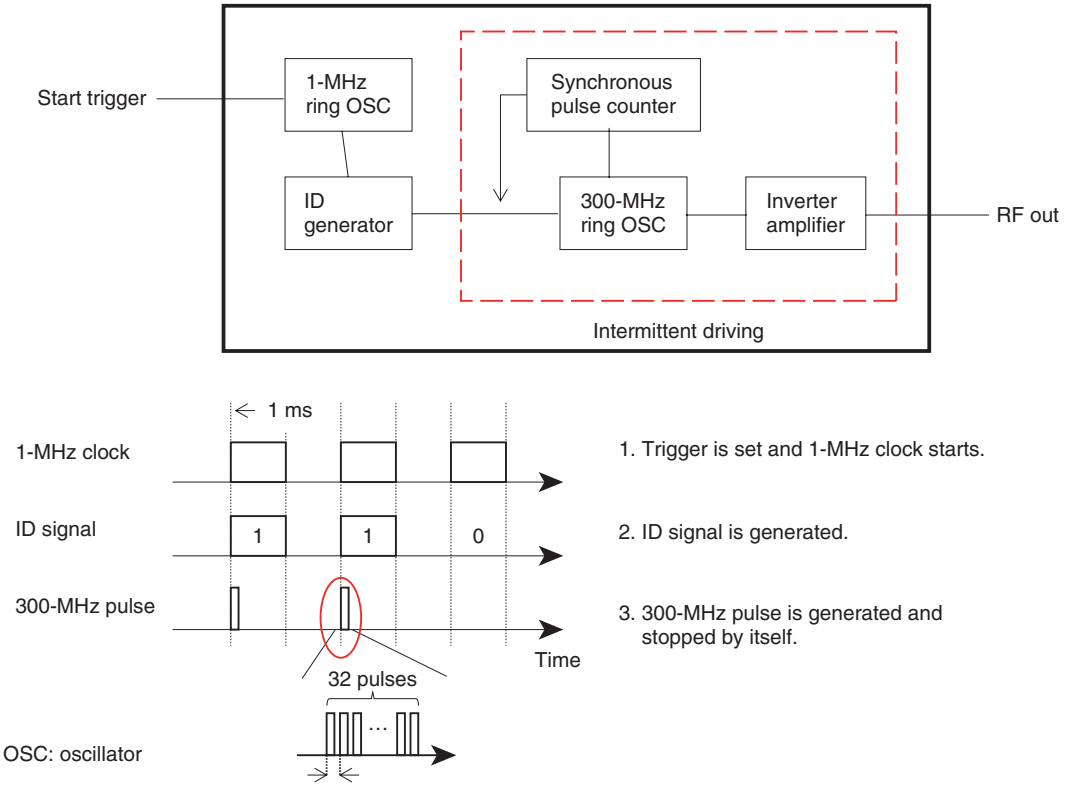


Fig. 5. Block diagram of proposed wireless transmitter.

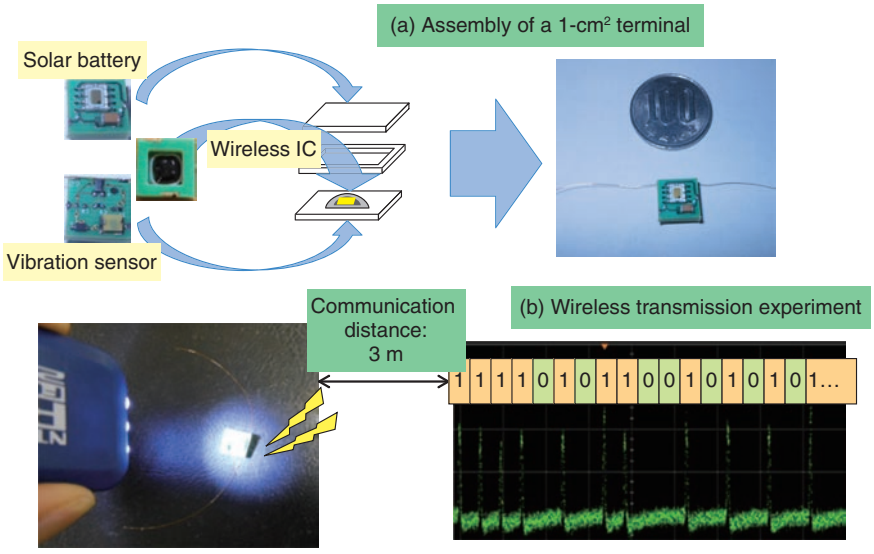


Fig. 6. Photographs of fabricated WSN and representation of bit data modulated by receiver.

A block diagram of the proposed wireless transmitter is shown in **Fig. 5**. It consists of a baseband ring oscillator for a data clock, an RF ring oscillator for a pulse generator, a pulse counter, an identification (ID) generator, and a driver amplifier. The ring oscillator is effective for achieving a quick startup. When the baseband oscillator starts, the ID signals are generated. While the signal is set to 1, the RF oscillator generates a pulse train. The pulse counter counts the number of pulses and stops the RF oscillator when the count reaches 32. After that, the RF circuits stop and consume no more power. The measured power consumption of 1-bit generation is 10 nJ/bit. This means that when we transmit 50 bits of "1" data in 1 s, the total power consumption is 500 nW.

3. Fabricated WSN

Photographs of a fabricated WSN are shown in **Fig. 6**. The configuration is also shown. The WSN has a solar battery, vibration sensor, wireless IC, antenna, and other devices. The total volume is 1 cm^3 with a small-wire dipole antenna. The 1-cm^2 printed circuit boards are stacked three-dimensionally to reduce the total size. The frequency band is set to 300 MHz, which means that no usage license is necessary under low output power conditions in Japan. The data rate is 1 Mbit/s and the bandwidth is 10 MHz. The transmitted data length is 36 bits including the preamble, fixed pattern, and ID. When the WSN detects sufficient vibration, it transmits the ID.

The measurement setup and results are also shown in Fig. 6. The WSN was charged with solar energy, and the data signals were then transmitted when the vibrations were detected. The ID signals were strong enough for a receiver located 3 m away to detect them and to demodulate bit data.

4. Concluding remarks

The ultrasmall WSN powered by an energy harvester is expected to lead to new services. In this article, we introduced nanowatt circuit technologies for sensing and wireless circuits. The fabricated 1-cm^3 WSN successfully transmitted an ID a 3-m distance using only solar energy.

In future, we will attempt to fabricate a much smaller WSN that can transmit signals a much longer distance using less energy; such an achievement would allow any object in the world to be connected to a network.

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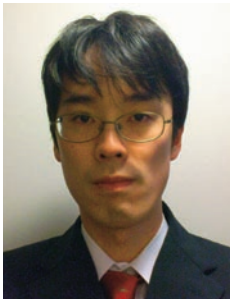

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Low-power-consumption Sensor Interface Terminal for Telemetry Applications

Toshihiko Kondo and Mitsuru Harada

Abstract

We have developed a sensor interface terminal with low power consumption that enables various communication terminals to accommodate several sensors. In this article, we describe the concept of the interface terminal and the technologies applied to achieve low power consumption. We also give an overview of a prototype terminal and report the results of its demonstration in an actual environment.

1. Introduction

1.1 Telemetry

Telemetry is the collection of data from various measurement instruments through communication lines. One of the most common applications of telemetry is the remote reading of gas, water, and electricity meters. A telemetry system recently introduced in Japan for reading liquefied petroleum gas meters is now used for more than 6 million customers [1]. The system has also been applied to inventory control of vending machines, parcel delivery management, and temperature monitoring in greenhouses to improve efficiency, service, and safety [2].

The system is an M2M (machine-to-machine) service that provides communications between a server and sensors without any manual input. It primarily uses subscriber telephones and optical lines as communication lines in wired systems and the 3G (third-generation) network, PHS (personal handy-phone system), and specified low-power radio [3] in wireless systems. These communication lines are selected to match the installation environment and utilization goals.

1.2 Importance of sensor interface

NTT Microsystem Integration Laboratories has developed low-power terminals, interfaces, and sensor circuits for ubiquitous sensor terminals. We applied these elemental technologies in a terminal used for remote reading of gas meters and for visualizing electricity consumption, and we conducted trials to evaluate the sensor terminal performance [4].

A ubiquitous sensor terminal mainly comprises a communication unit, interface unit, and power supply unit, as shown in **Fig. 1**. The communication unit controls connections with communication lines and accommodates various sensors through the interface unit. The power supply unit is usually equipped with a primary or secondary battery. In addition, a power generator such as a solar cell is sometimes installed to effectively use renewable energy. It is impractical to fabricate a terminal with a unique composition because the requirements for these units strongly depend on the target application, and they therefore must be generalized so they can be used in diverse conditions. Therefore, the sensor interface terminal, which mediates between a communication terminal and sensors, is very important for connecting various types of communication lines to various types of sensors.

The next section describes a sensor interface terminal that we developed based on NTT's established technologies and knowhow.

2. Sensor interface terminal

2.1 Overview

We established three main control technologies for the sensor interface terminals. The first is circuit

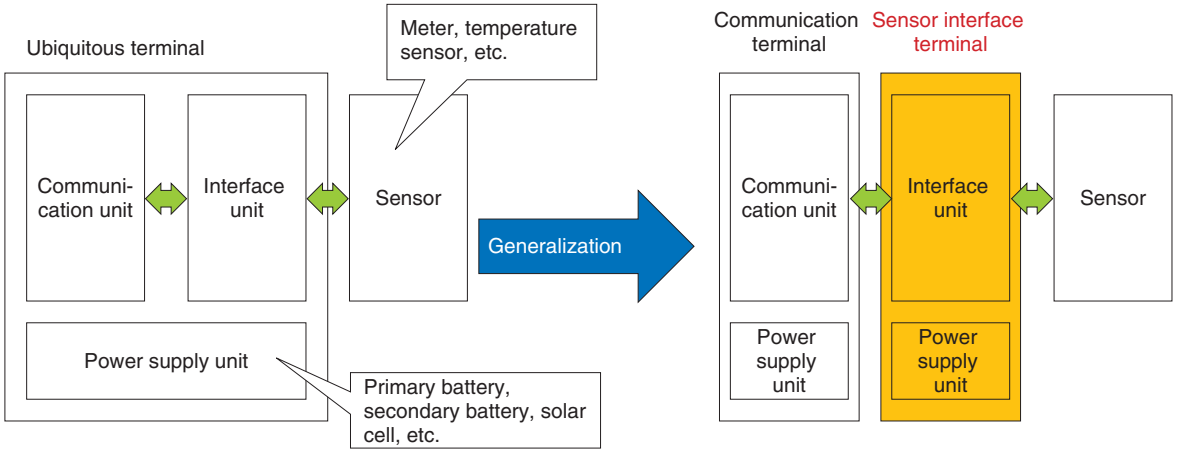

Fig. 1. Concept of sensor interface terminal.

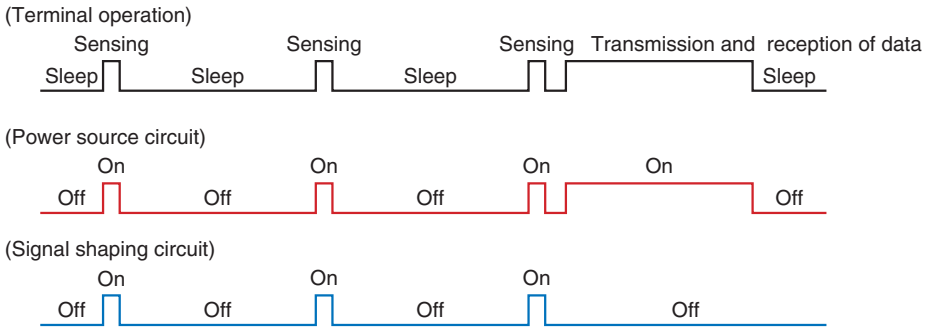

Fig. 2. Operation profile of terminal.

control, which involves intermittent operation of each circuit and an interruption control. The second is data-transmission control, which reduces the frequency of transmission to a minimum by combining immediate transmission and block transmission. The third is adaptive retry control, in which data transmission is retried according to an algorithm that is matched to a characteristic or condition of a communication line. The use of these technologies leads to a battery life from five to ten years in a sensor interface terminal.

2.2 Circuit control

In telemetry terminals, a battery life of more than a few years is generally required in order to cope with added installation sites and to reduce maintenance costs. For example, the communication units in the terminals used for remote reading of gas and water meters have very low power consumption and are powered by a battery rather than by utility power. Therefore, an equivalent battery life is required in the sensor interface terminal, which is one of the system components. To meet this requirement, the accumulated operation time is minimized by finely controlling the operation time of each circuit block, in particular, the power supply circuit and signal shaping circuit, which have relatively high power consumption. The operation profile of the terminal is shown in **Fig. 2**. The terminal activates both the power supply circuit and the signal shaping circuit when it obtains sensor data. The terminal turns on only the power supply circuit when it communicates with a communication terminal. Furthermore, we minimized the power consumption of the microcontroller, which controls the entire terminal, and that of the interface circuit using sleep control and an event-driven

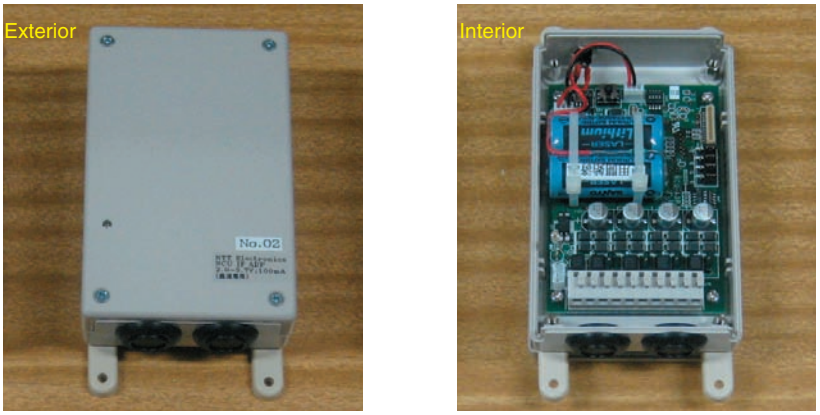

Fig. 3. Photographs of prototype terminal.

wake-up function. This control is effective because the power consumption in the sleep period strongly affects the total power consumption of the terminal when communication occurs very infrequently.

2.3 Data-transmission control

In less demanding applications such as remote meter reading, reducing the frequency of communication is effective for reducing power consumption. By contrast, in demanding applications such as alarm systems, realtime performance is very important. In some cases, a small number of data-transmissions is desirable, for example, when a fee for the communication line is charged according to the amount of transmitted data. Transmission control that takes these factors into consideration is necessary.

We established a data-transmission method to satisfy the above requirements. The terminal accumulates sensing data in its internal memory and manages them as bundled data. The terminal transmits the bundled data in a lump. The significant decrease in the overhead of data and packets reduces memory consumption, the amount of data that is transmitted, and the frequency of transmission, resulting in low power consumption. For event-driven data originating from the terminal, the terminal transmits sensing data individually without bundling to ensure realtime performance.

2.4 Adaptive retry control

The appropriate retry control must be selected according to the application because the communication line that is used normally depends on the application. Retry control is required in order to avoid collisions between transmitted data and to minimize delay. It is important to retry data transmission when the carrier is not busy when using specified low-power radio as the communication line.

We devised a method that adaptively alters the retry interval and timing according to the properties and condition of the communication line, which are estimated from the time taken to establish a link and to transmit data. An optimized retry algorithm enables the terminal to transmit data efficiently and reduces the time for retries and the total time for completing a series of data transmissions, which results in less power waste.

3. Demonstration in actual environment

3.1 Prototype terminal

We applied the technologies explained in section 2 to experimentally produce a sensor interface terminal that can be accessed by a communications terminal for remote gas meter reading. Photographs of the prototype terminal are shown in **Fig. 3**, and the specifications are listed in **Table 1**. The terminal has one communication interface and four sensor ports as input/output interfaces for external devices. This enables connection with various communication terminals in order to accommodate several clamp-type alternating current sensors (CTs) and conventional sensors with analog outputs. The ability to handle up to four sensors expands the range of potential applications. Here, we selected an interface that conforms to gas industry standardization as the communication interface. The terminal operates for five to ten years with a primary lithium battery as the power supply.

Table 1. Specifications of prototype terminal.

Communication interface	8-bit interface (standardized in gas industry)
Measurement range of alternating current	Below 500 A
Range of inputs from sensor equipment	DC 4–20 mA
Number of sensor ports	4
Data accumulation interval	30 minutes
Dimensions	125 (W) × 80 (H) × 32 (D) mm
Weight	Approximately 240 g
Power supply	Primary lithium battery
Battery life (estimated)	5–10 years

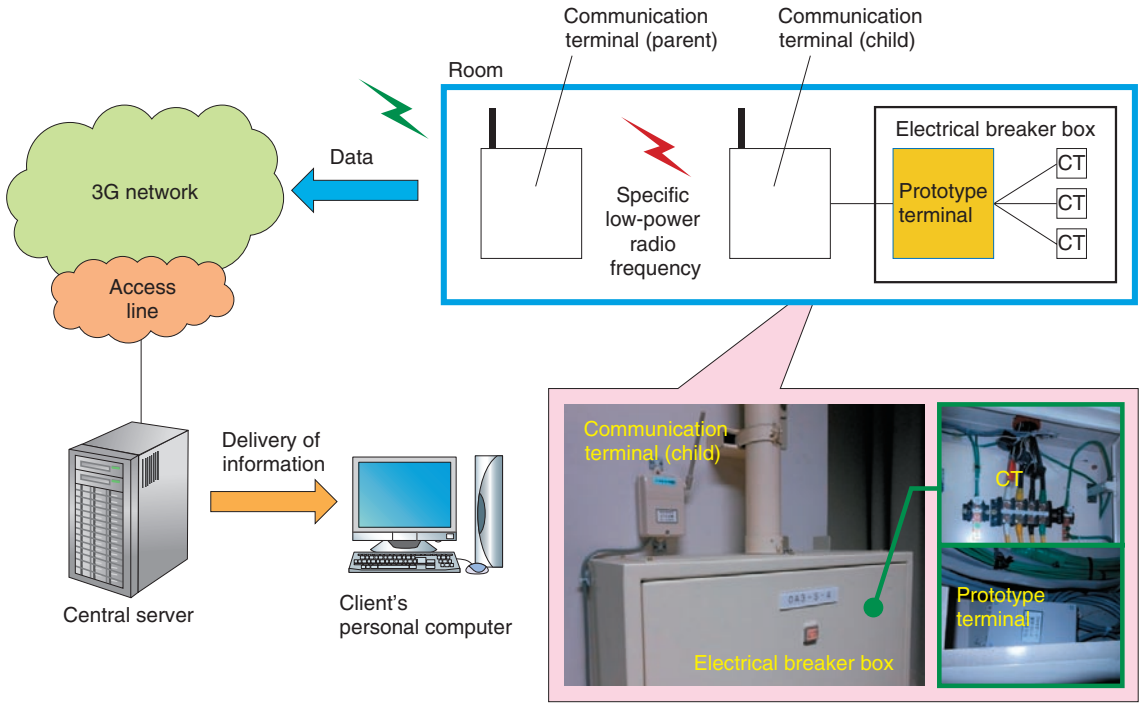

Fig. 4. System configuration for demonstration.

The long battery life makes these terminals good choices for installation in places without access to utility power.

3.2 Visualization of electricity consumption

We have been demonstrating the visualization of electricity consumption using the prototype terminal at the NTT Atsugi R&D center since August 2012. The system configuration used for the demonstration is shown in **Fig. 4**. The prototype terminal and three CTs are installed inside an electrical breaker box inside a room; a communication terminal with a radio is placed outside each breaker box. Seven terminals were installed in total. The communication terminals we used were commercial terminals for remote gas meter reading [5]. They consisted of a parent terminal and child terminal. The former communicates with the latter using specified low-power radio in the 429-MHz band and communicates with a central server through the 3G network and the access line. After the central server gathers and processes sensor data, it delivers information such as electricity consumption to the client PC (personal computer). An example of the observed information is shown in **Fig. 5**. This

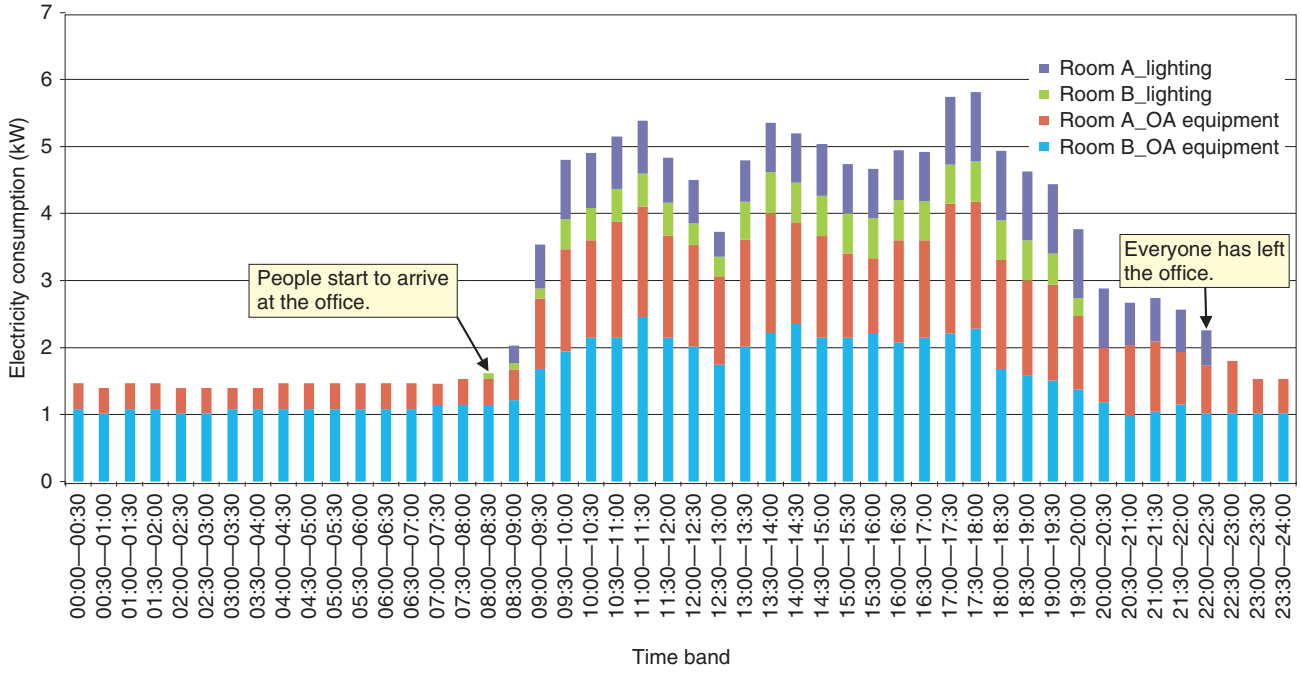

Fig. 5. Example of observed information.

system visualizes the time course of electricity consumption of every circuit in each room in detail. This makes it easy to see where energy-saving actions can be promoted. In addition, we can understand various tendencies from this information. For example, electricity consumption of lighting and office automation (OA) equipment respectively indicates the presence and activity of people, whereas the electricity consumption of OA but not of lighting indicates that people are not present.

4. Conclusion

We introduced a sensor interface terminal that can be used for various telemetry applications as an example of a ubiquitous sensor terminal that uses NTT's core technologies to achieve low power consumption. We demonstrated that the terminal allows conventional sensors to be easily connected to networks. We expect that this terminal will provide a platform that can flexibly accommodate various applications. In the future, we will promote research and development to expand the interface functions and add new functions to extend the range of applications.

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Vibrational Energy Harvesting with Microelectromechanical System Technology

Kazuyoshi Ono, Norio Sato, Tomomi Sakata, Junichi Kodate, and Yoshito Jin

Abstract

This article introduces a system for converting ambient vibrational energy to electrical energy using a microelectromechanical system (MEMS). A novel slit-and-slider structure is proposed as a way to miniaturize small sensor terminals. The results obtained with this system are expected to pave the way to designing and fabricating small vibrational energy harvesters.

1. Introduction

Different sources of energy such as thermal energy, light energy, and vibrational energy exist in the ambient environment. Energy harvesting is a technology for capturing minute amounts of energy from one or more of these naturally existing energy sources in order to generate electrical energy from it and store it for later use. The harvesting of vibrational energy has been an area of particular interest and has been intensively studied because vibrational energy exists almost everywhere in our living environment [1]. Recent progress in various low-power-consumption technologies in the semiconductor field has made it possible to drive various circuits or devices with a tiny amount of energy. Consequently, the utilization of energy sources in the ambient environment has become a realistic possibility. Some groups in our laboratory have been researching sensor terminals and their low-power circuits for future ubiquitous sensor networks [2]. One of the fundamental technologies for these terminals that our group has been investigating is vibrational energy-harvesting technology using a microelectromechanical system (MEMS). This article describes the principle of converting energy from vibration, and reports on the fabrication and basic characteristics of a novel structure with a MEMS.

2. Fundamental process of energy harvesting with electrostatic conversion from vibrational energy

Three types of energy conversion are possible when harvesting vibrational energy: electrostatic, piezoelectric, and electromagnetic [3]. Because we desire a power supply for various integrated circuits in a small sensor terminal, we chose electrostatic conversion because it is compatible with a planar process. An electrostatic energy harvester exploits the phenomenon of electrostatic induction by a dielectric. An electret is a suitable dielectric material because it can be charged to a high voltage and can hold the voltage semi-permanently on its surface. Electrets are used in many applications such as condenser microphones and air filters.

The fundamental setup of the vibrational energy harvesting process using electrostatic induction with an electret [4], [5] is shown in **Fig. 1**. When negative charges are applied to the electret, positive charges are induced on a fixed electrode and a movable electrode (Fig. 1(a)). When the movable electrode plate is displaced by an external vibration in the direction of the arrow, some of the positive charges are moved from the fixed electrode to the movable one, and then current is generated through the external load (Fig. 1(b)). When positive charges are applied to the

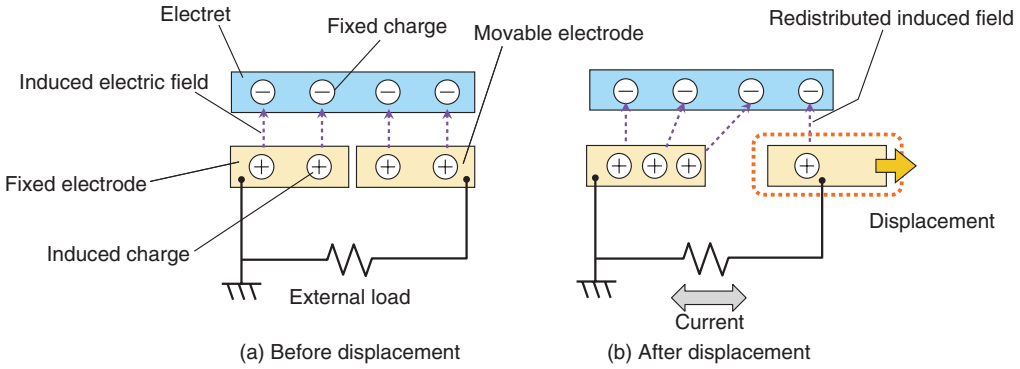


Fig. 1. Principle of vibrational energy harvesting by electrostatic induction with electret.

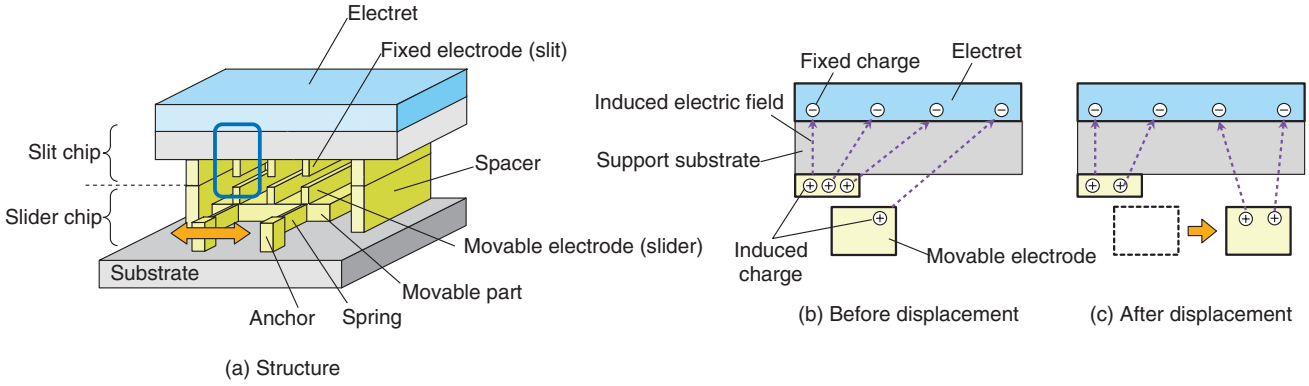


Fig. 2. Slit-and-slider structure.

electret, negative charges are induced on the electrodes. This current is expressed as

$$I = \frac{dQ}{dt} \tag{1}$$

where, I, Q, and t are current, charge, and time. Assuming that the fundamental structure is an electrostatic capacitor model, we rewrite eq. (1) as

$$I = V\frac{dC}{dt} = \varepsilon V\frac{d}{dt}\left(\frac{S}{d}\right), \tag{2}$$

where, V, C, ε, S, and d indicate voltage, capacitance, permittivity, the area of capacitance, and the gap of capacitance. The current increases as the gap of the structure becomes smaller, the area of the structure becomes larger, the constant of the electret material becomes higher, and the voltage of the electret becomes higher.

3. Novel structure

3.1 Design

The novel structure we devised [4], [5] is shown in **Fig. 2**. This structure, called a slit-and-slider structure, consists of an electret, a slit chip, which has fixed electrodes and physically supports the electret, and a slider chip, which has a movable electrode displaced by external vibration (Fig. 2(a)). The slit and slider chips are connected by a spacer to create a suitable gap between the fixed and movable electrodes. An illustration of part of the structure after the movable electrode moves is shown in Figs. 2(b) and (c). When negative charges are applied to the electret, positive charges are induced in the fixed and movable electrodes by an electric field that passes through the substrate (Fig. 2(b)). When the movable electrode is displaced to the right, some positive charges in the fixed electrode move to the movable electrode

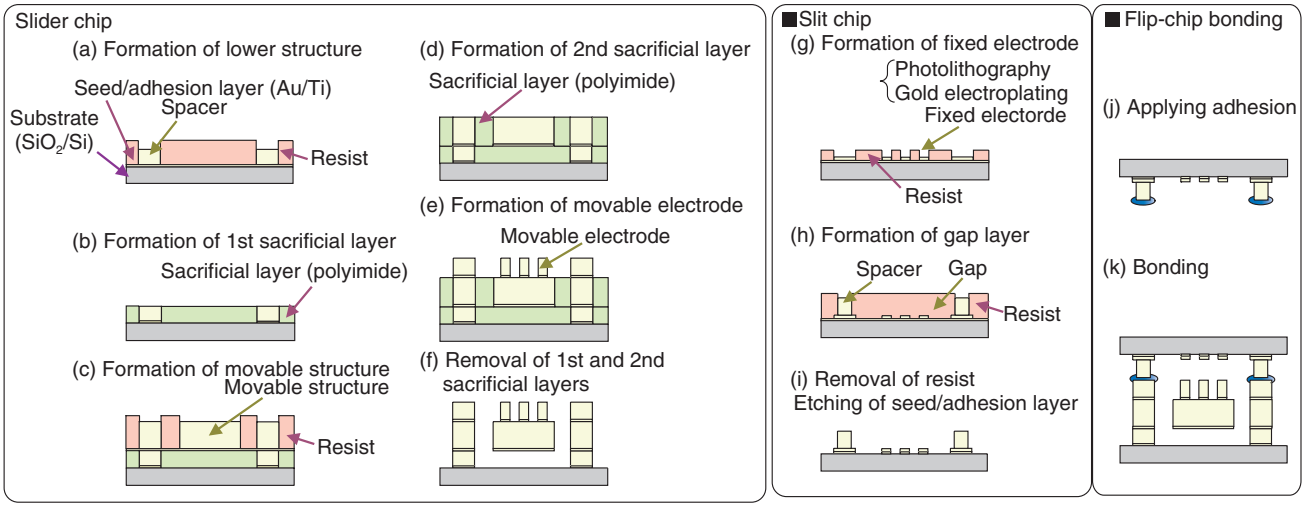
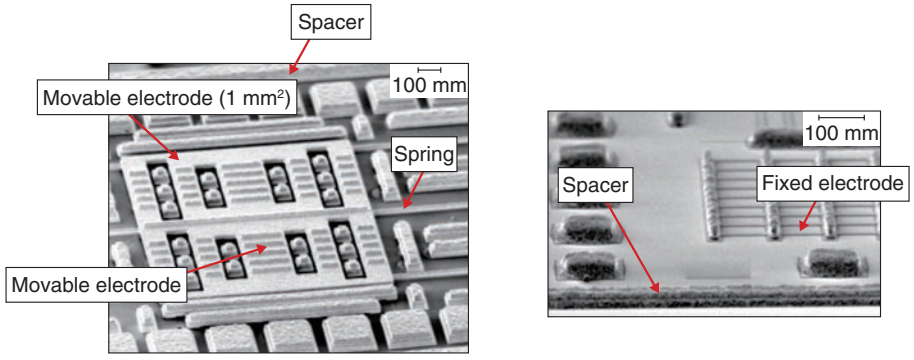


Fig. 3. Fabrication process.



(a) Slider chip (b) Slit chip

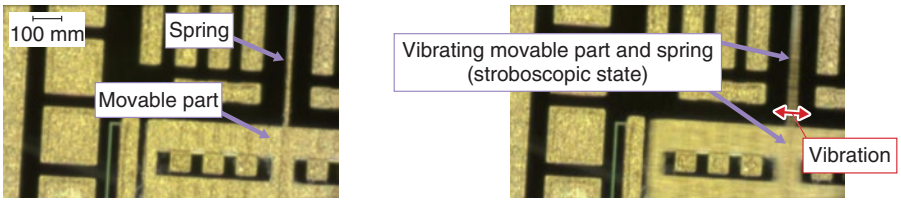
Fig. 4. Photographs of fabricated chips.

(Fig. 2(c)). AC (alternating current) between the fixed and movable electrodes is generated by the vibration of the movable part.

3.2 Fabrication process

The fabrication process for the device structure is based on thick-electroplating technology [6]. The fabrication process flow for the slit-and-slider structure is shown in **Fig. 3**. For the slider chip, first, the lower structures of the movable plate, for example, the lower interconnections, are formed on the substrate by gold (Au) electroplating (Fig. 3(a)). Next, the lower structures are planarized with photosensitive polyimide (Fig. 3(b)). The polyimide is a sacrificial layer that is removed later. Then, other parts of the movable plate and spacer are formed by repeating the electroplating and planarization steps (Figs. 3(c) to (e)). This stacking process simplifies the fabrication of the multilayered structure. Finally, the sacrificial layers are removed by dry ashing (Fig. 3(f)). The slit chip is fabricated using the same process. To bond the two chips, silver paste is applied to the walls of the slit chip, which is then flipped over and hot-pressed against the slider chip.

Images of fabricated slider and slit chips are shown in **Fig. 4**. The images were taken before the flip-chip bonding. Different elements for the slit-and-slider structure were fabricated on the substrate by stacking



(a) External vibration: OFF (b) External vibration: ON

Fig. 5. Optical microscopy images (a) without and (b) with external vibration applied.

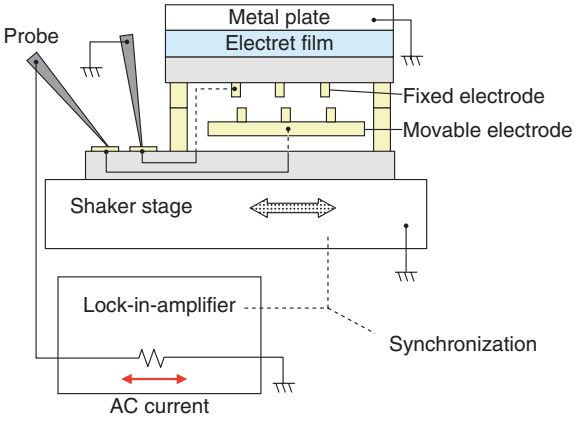


Fig. 6. Experimental setup for current generation.

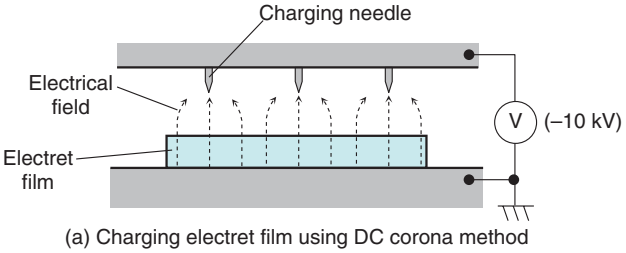
multiple layers. The movable plate is 1 mm^2 in size and 20 μm in thickness, which makes it the smallest structure ever reported for an energy harvester with electrostatic induction.

Close-up views of a movable plate on a chip without and with external vibration are shown in **Figs. 5(a)** and **(b)**, respectively. When the movable plate moves vigorously because of the external vibration, a stroboscopic effect is observed for the movable plate and spring.

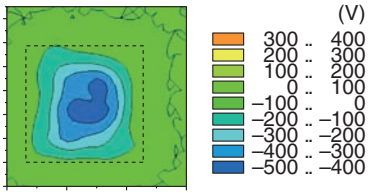
4. Energy harvesting experiment

A schematic diagram of the experimental setup for current generation is shown in **Fig. 6**. The output from the movable electrode was connected to the input of a lock-in amplifier. The lock-in amplifier detects components with the same frequency as an input vibration reference signal. The surface of the electret was attached to the top of the slit chip, and the electret was fixed with a metal plate. The fixed and movable electrodes were interconnected separately outside the walls of the structure. The fixed electrodes and metal plate were connected directly to the ground. The frequency of external vibration was swept upwards, whereas acceleration was kept constant at 1 m/s^2.

In this experiment, we used ethylene-tetrafluorinated ethylene copolymer (ETFE) film as an electret, because this material has long-term stability for holding charges [7], [8] and a good record of use in commercial products and applications [9]–[12]. The experimental setup for charging the electret film is shown in **Fig. 7**. The film was DC (direct current)-corona-discharged between a grounded electrode and high-voltage needle electrodes in this apparatus (Fig. 7(a)). The discharge was applied at –10-kV bias voltage at room temperature. The surface potential distribution of the charged film, which was set on the automatic two-axis stage, was measured with an electrostatic voltmeter. The measured potential distributions of the surface for each electret film are shown in



(a) Charging electret film using DC corona method



(b) Potential distribution on surface of ETFE film

Fig. 7. Charging of electret film.

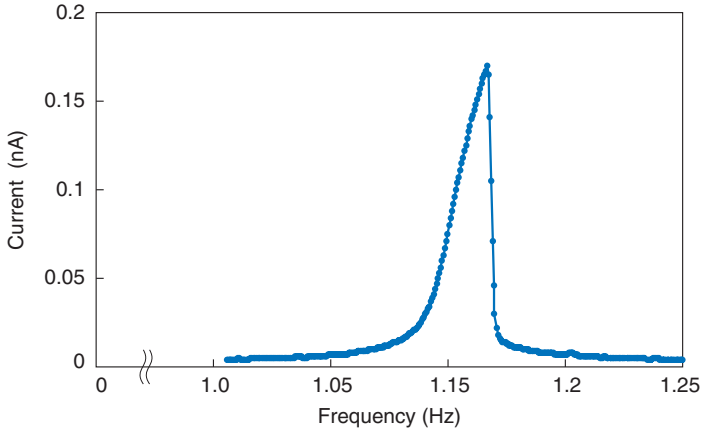


Fig. 8. Current generation results.

Fig. 7(b). The surface potentials are about –450 V at minimum.

The current generation is shown in **Fig. 8**. The AC current is dependent on frequency. The current shows a peak at around 1.15 kHz. The maximum value is 0.17 nA at 1.17 kHz. This behavior coincides with the observation of the frequency characteristic of the movable part before flip-chip bonding, as shown in Fig. 5(b). Thus, the peak intrinsically comes from the resonant vibration. This result confirms that the vibrational device generates current with the electret.

5. Conclusion

We investigated a technology for vibrational energy harvesting using a novel slit-and-slider structure with electrostatic induction. We demonstrated through experiments that AC current was generated by external vibration and the electret. The maximum current was 0.17 nA at 1.17 kHz of external vibration with a magnitude of acceleration of 1 m/s^2. These experiments show the potential of vibrational energy harvesting. This promising technology is expected to lead to the development of an energy harvester and sensor network terminals.

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Integrated Silicon-based Optical Interconnect for Fast, Compact, Energy-efficient Electronic Circuit Systems

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Abstract

The performance of electronic circuit systems is now reaching saturation because of restrictions on the bandwidth, integration density, and power consumption of electronic interface devices. In this article, we present high-density chip-to-chip optical interconnects based on silicon photonics technology, which has the potential to solve these critical problems.

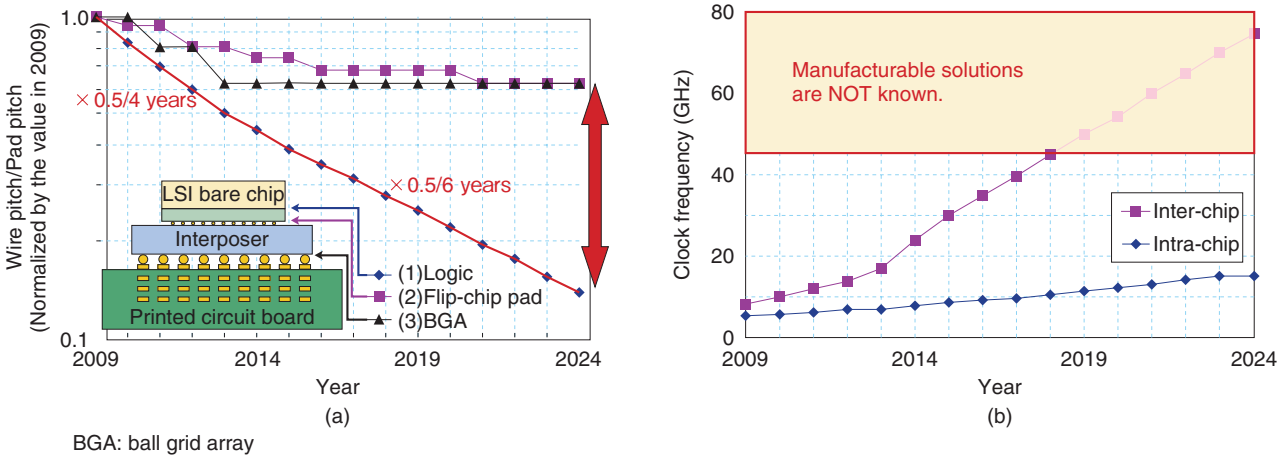
1. Optical interconnects in electronic circuit systems

The information and communications industries are now facing an explosive increase in information processing capacity in order to support the distribution of heavy loaded rich content and the growing use of high-performance mobile terminals.

The extensive construction of broadband network systems and huge datacenters has been carried out in order to cope with this information explosion. These large-scale information processing systems use an infinite number of electronic circuits, and it is therefore critical to improve their performance and reduce their power consumption. For example, the bandwidth of chip-to-chip interconnects between LSIs (large-scale integrated circuits) will double every two years and reach 1 Tbit/s in the mid 2010s and 10 Tbit/s in 2020 [1].

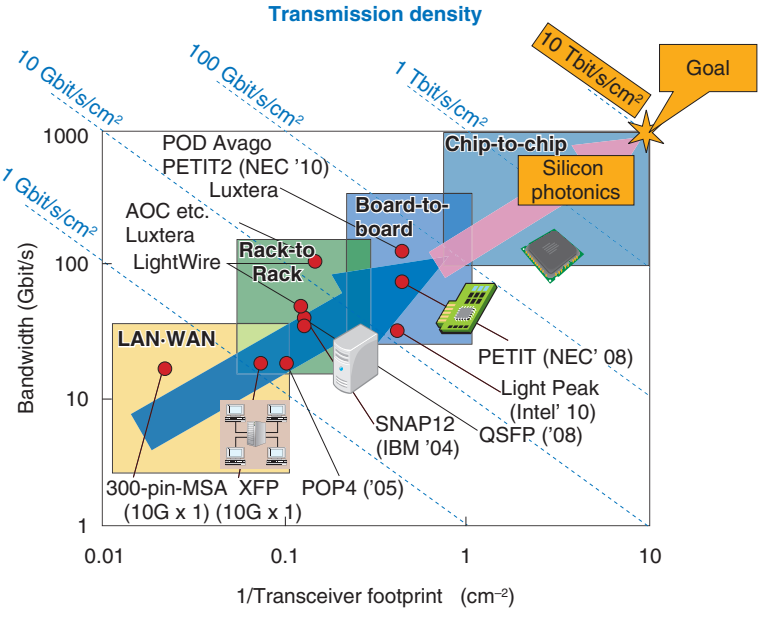
However, from the viewpoint of size and power consumption, such broadband interconnects cannot be achieved with conventional electrical wiring. The trend in the distance separating neighboring electrical wirings, which would determine the size of data interconnect systems [2], is shown in **Fig. 1**. For intra-chip interconnects, the separation can be reduced thanks to advances in microfabrication technology. For chip-to-chip interconnects, however, the separation must have some lower limit because the separation is determined by the geometrical structure of the pads and pins of LSIs, through which the LSIs are connected to printed circuit boards. Figure 1(b) shows the trend in signal frequency, which directly affects the power dissipation in electrical wiring. By the late 2010s, when the frequency is expected to reach 40 GHz, conventional electrical wiring will not be able to provide any practical solutions [2].

To solve these interconnect-related problems in electronic circuit systems, many organizations have developed optical interconnect technology. The relation between interconnect bandwidth and the footprint of interconnect modules [3] is shown in **Fig. 2**. Optical interconnect modules have conventionally been based on discrete photonic devices made of compound semiconductors and developed for applications in LANs (local area networks) and WANs (wide area networks) and for inter-rack and on-board interconnects. However, constructing a chip-to-chip interconnect system is very difficult with conventional photonic technology because it requires ultra-high-density photonic device integration. Moreover, it is also very difficult with conventional photonic



BGA: ball grid array

Fig. 1. Trends in (a) wiring pitch and (b) signal frequency for chip-to-chip interconnections.



AOC: active optical cable
MSA: multi-source agreement
POP4: Post Office Protocol version 4
QSFP: quad small form-factor pluggable

Fig. 2. Trends in optical interconnection technology.

technology to converge photonics and electronics, which is one of the most important requirements in the optical interconnects. This is because materials, device sizes, design schemes, and fabrication processes in conventional photonic technology are quite different from those of electronics.

To solve these problems in conventional photonic technology and to construct a chip-to-chip optical interconnect system, we have developed a system using silicon photonics technology. This system can achieve high-density photonic device integration and has the potential for photonic-electronic convergence.

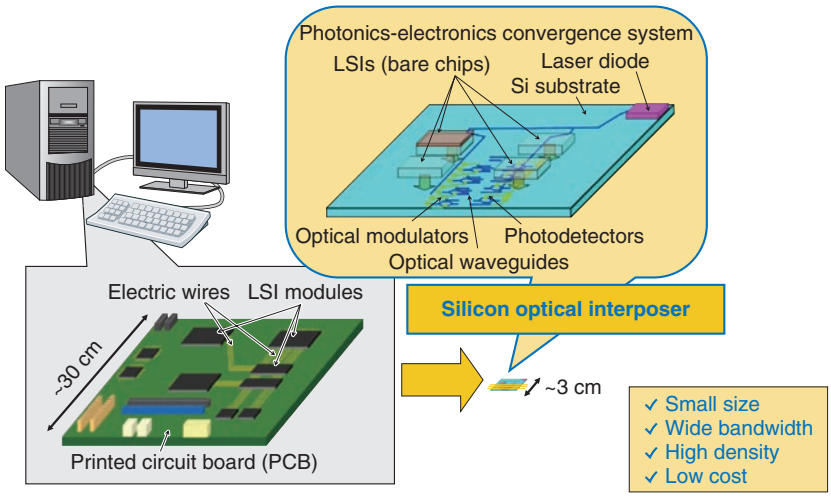


Fig. 3. Concept of chip-to-chip optical interconnection based on silicon photonics technology.

2. Concept of high-density optical interconnect system

A conceptual image of the high-density chip-to-chip optical interconnect system, or ultracompact optical interposer, is shown in **Fig. 3** [3]. Laser diodes (LDs), optical modulators, and photodetectors (PDs) are integrated on a single silicon substrate and optically linked to each other by silicon optical waveguides. Bare LSI chips are mounted on the substrate and electrically connected to the optical modulators and PDs on the substrate by flip-chip bonding. Silicon photonics technology makes photonic devices ultracompact, and their integration density can therefore be significantly improved. The compact and high-density photonic device integration provides a compact optical interconnect system with large bandwidth and low power consumption. Moreover, CMOS (complementary metal-oxide semiconductor) electronics technology is used for most of the design and fabrication processes, which makes it easier to integrate discrete optical parts in the design and assembly processes. Thus, we can significantly reduce the costs of design and fabrication of integrated photonic devices.

This technology will make it possible to achieve integrated silicon optical interconnect circuits with 10-Tbit/s/cm^2 bandwidth in fiscal year 2013.

3. Fabrication of integrated silicon-based optical interconnect circuits

A photograph of the integrated silicon-based optical interconnect circuits we fabricated in 2010 [4] is shown in **Fig. 4**. The fabricated chip is 4.5 × 5 mm. A 13-channel (ch) LD array, silicon optical modulator array, and germanium (Ge) PD array are constructed on this chip, and these photonic devices are connected by silicon photonic wire waveguides. These devices are fabricated on a 4-inch silicon on insulator (SOI) wafer using a state-of-the-art fabrication process that is compatible with that for electronic circuits.

Cross-sectional structures of the photonic devices on the chip are shown in **Fig. 5**. The SOI layer, which forms the core of the silicon (Si) waveguide, is 200 nm thick. This SOI layer was used to fabricate 600-nm-wide silicon waveguide cores by electron-beam lithography and dry etching. Silicon optical modulators with a lateral p-i-n electronic structure were fabricated by implanting boron and phosphor ions. The silicon optical modulator is only 340 μm long, which is a few tenths the size of conventional ones made of lithium niobate crystals. Ge PDs were also fabricated by growing a Ge layer on the SOI layer and implanting boron ions into the Ge. The high-purity Ge layer was grown only in the region designed for the PDs by using the UHV-CVD (ultra-high vacuum chemical vapor deposition) method.

A silica overcladding layer was deposited on these optical modulators and Ge PDs by electron cyclotron resonance plasma-enhanced chemical vapor

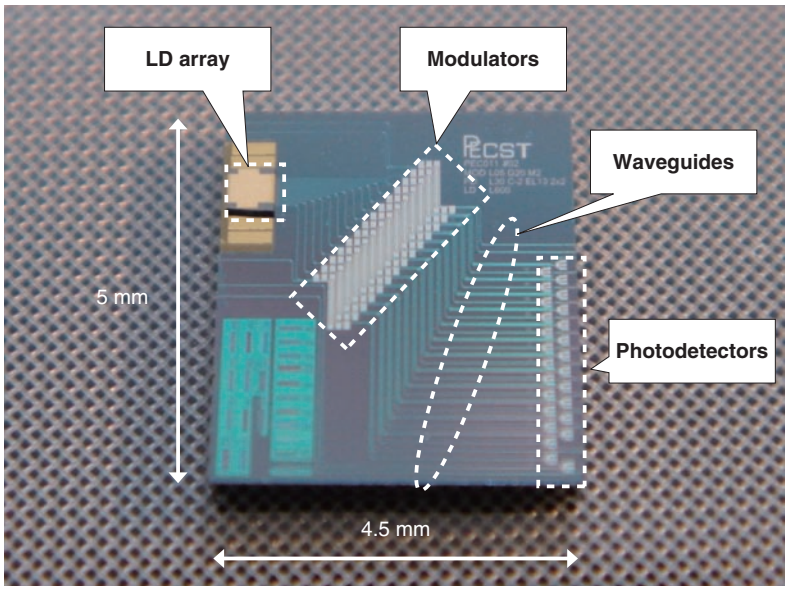


Fig. 4. Photograph of integrated silicon-based optical interconnect circuits.

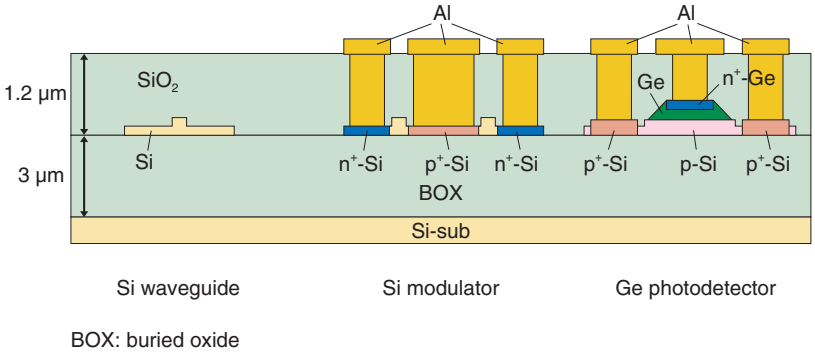


Fig. 5. Cross-sectional structures of photonic devices.

deposition (ECR-PECVD). The ECR-PECVD method allows silica layers to be deposited at temperatures below 200°C, which means we can form the silica overcladding layer without damaging the modulators and photodetectors underneath it. The silicon chip with the waveguides, modulators, and PDs was fabricated by NTT Advanced Technology Co. Waveguide facets and stages for LDs are formed on the fabricated chip by dry etching. Then, a 13-ch LD chip was mounted on the chip using a unique passive alignment method developed by PETRA (Photonics Electronics Technology Research Association) [5]. The wavelength of the LDs is in the 1.55-μm infrared band, which is widely used in telecommunications applications.

4. Performance of integrated silicon-based optical interconnect circuits

First, we present the performance of single devices fabricated on the chip. The measured optical attenuation performance of the Si modulator is shown in **Fig. 6**. The optical output power from the modulator was measured while applied voltage to the p-i-n structure of the modulator was swept. As shown in this figure, the $V_{\pi}L$ value, which represents the modulation efficiency of the modulator, is as small as 0.012 V • cm. A modulator with such a small $V_{\pi}L$

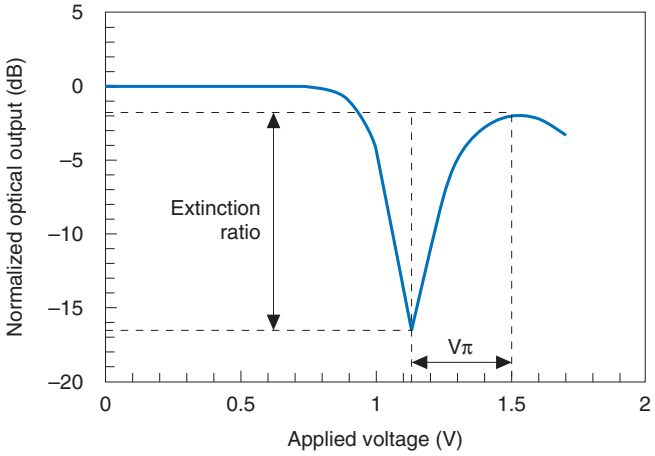


Fig. 6. Extinction performance of silicon optical modulator.

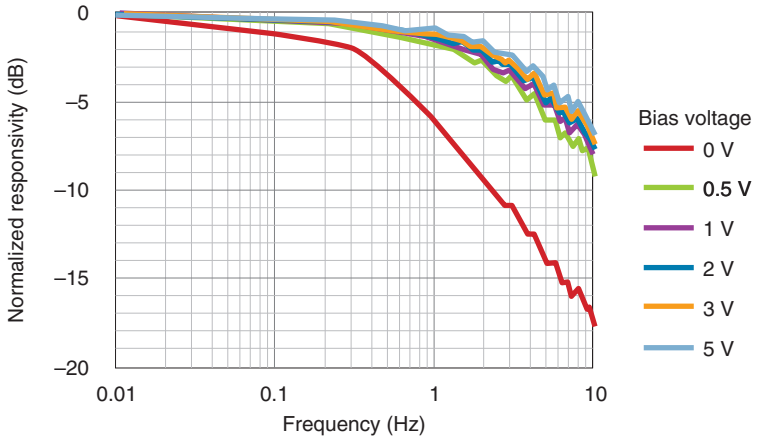


Fig. 7. Frequency characteristics of Ge PD.

achieves low-voltage optical modulation. The extinction ratio of optical power is about 15 dB, which is large enough for optical data transmission [4]. Although the 3-dB frequency bandwidth of the modulator is a few hundred megahertz, the device can be used in operations of a few gigabits per second by applying a pre-emphasized input. The measured frequency characteristics of a PD are shown in **Fig. 7**. The 3-dB frequency bandwidth is 4.2 GHz, which is sufficient for receiving data at a few gigabits per second [4].

Next, let us look at the experimental results for the simultaneous operation of LDs, modulators, and PDs integrated on a chip. The 13-ch array of LDs was driven by a single DC power supply, and the continuous wave optical power from each LD was guided to an optical modulator. Digital signal data from a pulse pattern generator were pre-emphasized by an electrical differentiator and then applied to the modulator. The voltage of signal input to the modulator was 3.9 V_{pp}. The modulated optical signal was guided to the PDs and converted to an electrical signal. The experiment was performed under an uncontrolled temperature condition. An eye pattern of the output signal from the PD for a 5-Gbit/s NRZ (non-return-to-zero) data stream is shown in **Fig. 8(a)**. The eye pattern is clearly open, which confirms the 5-Gbit/s data transmission capability in the on-chip integrated optical interconnection circuit [4]. No significant channel cross-talk was observed in the neighboring

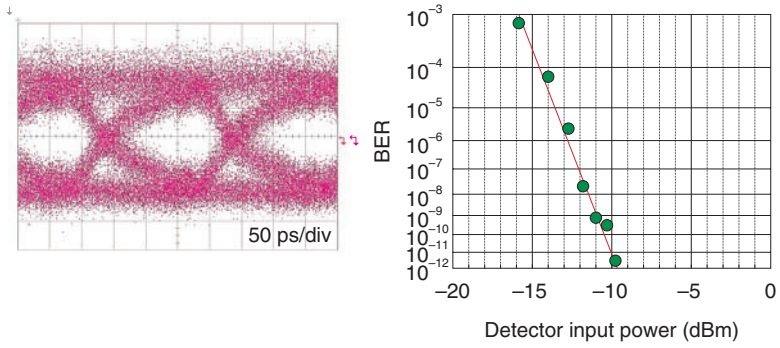


Fig. 8. Transmission performance: (a) eye pattern and (b) BER of received signals.

channels. The measured bit error rate (BER) in a 5-Gbit/s transmission operation is shown in **Fig. 8(b)**. A BER of less than 10^{-12}, or an error-free operation, was confirmed when the detector input power was -9.5 dBm.

In this silicon-based optical interconnection circuit, the sum of the footprints of an LD, modulator, and PD, including electrode pads, is estimated to be 0.144 mm^2 per channel. Since 5-Gbit/s data transmission has been confirmed in one data channel, the transmission density of this optical interconnection system is estimated to be 3.5 Tbit/s cm^2. This is a new world record for transmission density in an optical interconnection using light sources.

5. Toward 10-Tbit/s/cm^2 interconnects

In order to achieve our target transmission density of 10 Tbit/s/cm^2, further improvement in the device performance and a reduction in the device size are necessary. For example, a 100% increase in operation speed and a 30% reduction in device size are required. To increase the operation speed, we have developed modulators with a side-wall grating structure. This structure improves optical confinement and reduces the width of the waveguide core, which directly contributes to increasing the modulation efficiency and speed. Moreover, we have developed PDs with MSM (metal-semiconductor-metal) electrode structures; these PDs also contribute to increasing the frequency bandwidth of the photodetector. To reduce the footprint of the LDs, we have developed a low-loss LD coupling structure and optical branches, which makes it possible to reduce the number of LDs while keeping the optical power per channel constant. Thanks to these improvements, we have already increased transmission density to 6.6 Tbit/s/cm^2 [6]. For this result, the electrode pads, which occupy half of the device footprint, were still large because it was necessary to use measurement probes for testing. However, in practical interconnect systems, we do not need such large pads for the testing; therefore, we can significantly reduce the area of the electrode pads to achieve a 30% reduction in the total device footprint.

With these improvements, we expect to achieve our final target, a 10-Tbit/s/cm^2 transmission density, in the near future.

Acknowledgment

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Mechanical Transfer of GaN-based Devices Using Layered Boron Nitride as a Release Layer

Yasuyuki Kobayashi, Kazuhide Kumakura, Tetsuya Akasaka, Hideki Yamamoto, and Toshiki Makimoto

Abstract

Nitride semiconductors are the preferential choice in various device applications such as optoelectronics and high-power electronics. These gallium nitride (GaN)-based device structures can be grown on sapphire, silicon carbide, and silicon substrates, but not on large, flexible, and affordable substrates such as polycrystalline or amorphous substrates. This article reports our research results that demonstrate that hexagonal boron nitride (h-BN) can form a release layer that enables the mechanical transfer of GaN-based device structures onto foreign substrates. Aluminium (Al) GaN/GaN hetero-structures and indium (In)GaN/GaN multiple-quantum-well (MQW) structures grown on h-BN-buffered sapphire substrates, ranging in area from 25 mm^2 to 4 cm^2, were mechanically released from the host substrates and successfully transferred onto other substrates. The electroluminescence intensities from the transferred light-emitting diode (LED) were comparable to or higher than those from a conventional LED on a low-temperature AlN buffer layer, indicating that the MQW preserved its original quality after the transfer.

1. Introduction

1.1 GaN semiconductor growth

Gallium nitride (GaN)-based semiconductors have a wide range of applications such as high-power devices for wireless communications, visible light sources for illumination, and ultraviolet light sources for sterilization. In general, GaN-based semiconductors have been grown on single-crystal sapphire substrates using a buffer layer, which can consist of low-temperature aluminium nitride (AlN) [1], low-temperature GaN [2], or aluminium oxynitride (AlON) [3]. However, high-quality GaN-based devices cannot be grown on polycrystalline or amorphous substrates even by using state-of-the art growth technologies such as metal-organic vapor phase epitaxy (MOVPE). The laser lift-off technique [4] enables the transfer of GaN-based devices from one substrate to another. However, it has some disadvantages, such as the need for laser lift-off equipment and a surface cleaning process to remove material residues after laser irradiation. Hence, there is a compelling need for a simple technique that requires neither chemical treatment nor additional equipment for the transfer.

1.2 Boron nitride as a release layer

Boron nitride (BN) is not a naturally occurring chemical compound; it was first synthesized by W. H. Balmain [5] in 1842. This compound has three main crystal structures: hexagonal boron nitride (h-BN), cubic boron nitride (c-BN), and wurtzite boron nitride (w-BN), which are respectively shown in **Figs. 1(a), (b)**, and **(c)**. C-BN has been extensively studied for high-temperature and high-power applications. W-BN has a metastable crystal structure. H-BN, whose crystal structure is graphite-like with lattice constants of a = 2.50 and c = 6.66 Å, is a promising material for optical device applications in the deep ultraviolet

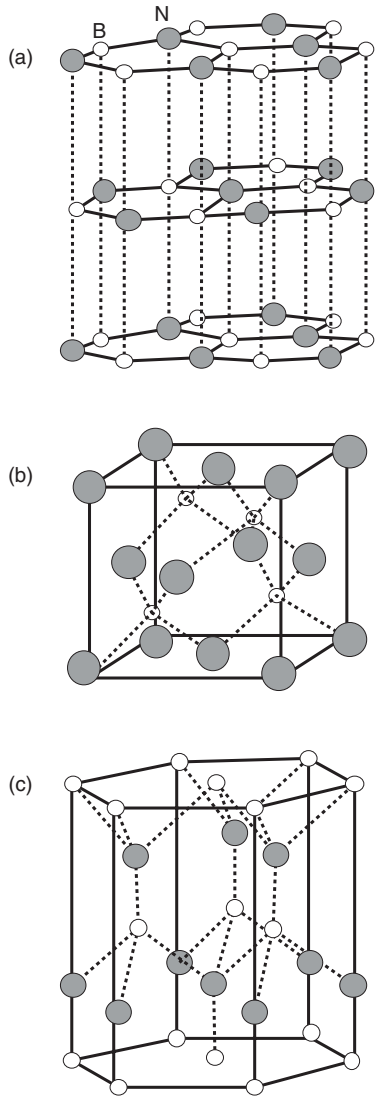

Fig. 1. Crystal structures of BN. (a) Hexagonal BN (h-BN), (b) cubic BN (c-BN), and (c) wurtzite BN (w-BN).

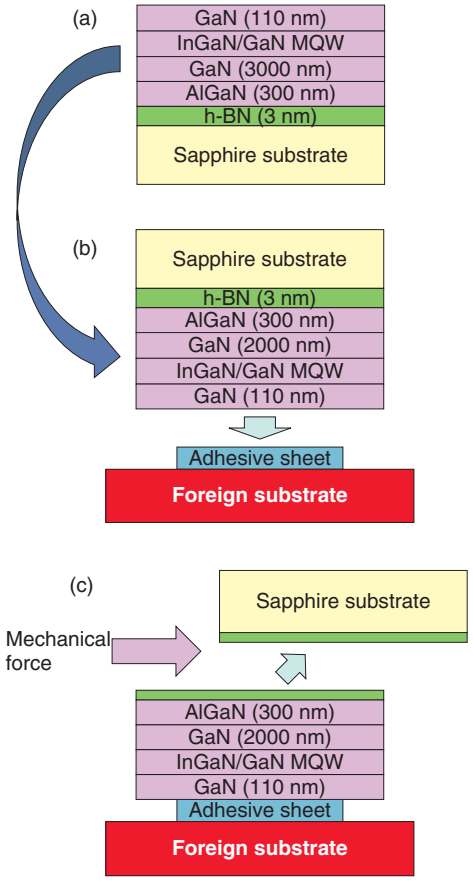

Fig. 2. Schematic illustrations of the MQW design, release, and transfer processes. (a) The MQW structure; (b) the MQW is placed on a foreign substrate; (c) the MQW is released from the host sapphire substrate.

spectral region. In addition, h-BN can potentially act as an ideal layer for mechanically releasing GaN-based devices from substrates because the layers in h-BN are bonded to each other by van der Waals attraction. Here, we use h-BN as a release layer, which enables us to release a GaN-based device structure from the substrate and transfer it to a foreign substrate mechanically [6]. Note that mechanically transferable GaN layers have been grown on zinc oxide (ZnO)-coated graphene layers [7], although there are size limitations, which presents a challenge. Polycrystalline BN films have also been used as buffer layers to grow GaN films on Si substrates [8], but this approach only resulted in polycrystalline GaN films.

2. Experimental

2.1 Growth process

The indium (In)GaN/GaN multiple-quantum-well (MQW) structure and the release and transfer processes are shown in **Fig. 2**. The h-BN release layer and the InGaN/GaN MQW structure were grown by MOVPE with hydrogen or nitrogen carrier gas. Triethylboron, trimethylgallium, trimethylaluminium, triethylgallium and trimethylindium were the group III source materials, and ammonia was the group V source. First, a single-crystal (0001) ultrathin h-BN layer with a thickness of 3 nm was grown on a (0001) sapphire substrate [9], [10]. The orientation

relationship between the substrate and the h-BN was $(0001)_{\text{h-BN}} \parallel (0001)_{\text{sapphire}}$. This indicates that the plane of boron and nitrogen was parallel to the substrate surface. Then, the InGaN/GaN MQW structure was grown on the h-BN release layer (Fig. 2(a)). The single-crystal h-BN layer works as the release layer. A flat single-crystal GaN layer can be grown on a single-crystal AlGaN or AlN layer on the h-BN despite the large lattice mismatch and the structural difference between the graphite-like (h-BN) shown in Fig. 1(a) and wurtzite (AlGaN and AlN) shown in Fig. 1(c).

2.2 Transfer to foreign substrate

After the growth, we flipped the MQW structure upside down and put it on a foreign substrate via an adhesive sheet (Fig. 2(b)). In this case we used an indium sheet as the adhesive; adhesive tape or glue would also work. Next, we heated the structure to a temperature sufficient to heat-seal the indium to the sapphire and the MQW. Finally, the MQW structure was released from the host sapphire substrate by mechanical force and thereby transferred to the foreign substrate (Fig. 2(c)). We call this transfer method "MeTRe" (Mechanical Transfer using Release layer).

3. Results and discussion

3.1 Mechanical release of MQW structure

A micrograph of the transferred InGaN/GaN MQW structure, approximately 25 mm^2, is shown in **Fig. 3(a)**. The structure is positioned on the indium sheet attached to the foreign substrate, as illustrated in Fig. 2(c). We also successfully transferred an AlGaN/GaN heterostructure, approximately 4 cm^2, on the indium sheets. The size of the transferred area can be controlled by adjusting the adhesive sheet size. Some protrusions from the indium sheet, which are at the upper side of the structure, are discernible, indicating that the InGaN/GaN MQW structure with a thickness of about 3.5 µm is mechanically released from the host sapphire substrate. The surface of the indium sheet is seen through the transparent InGaN/GaN MQW. No cracks were observed in the upper half of the MQW structure, which suggests that the mechanical release process results in minimal crack formation.

3.2 XRD results

We performed X-ray diffraction (using a 2θ/ω configuration) for the transferred MQW structure to check the crystal quality after the transfer. The X-ray diffraction (XRD) pattern in **Fig. 3(b)** shows satellite peaks from the MQW up to the first order, along with those for GaN (0002) and AlGaN (0002), without any trace of a sapphire (0006) peak. X-ray diffraction of the InGaN/GaN MQW structure before the transfer shows satellite peaks from the MQW, and peaks of GaN (0002), AlGaN (0002), and sapphire (0006). This means that the MQW structure consisting of the

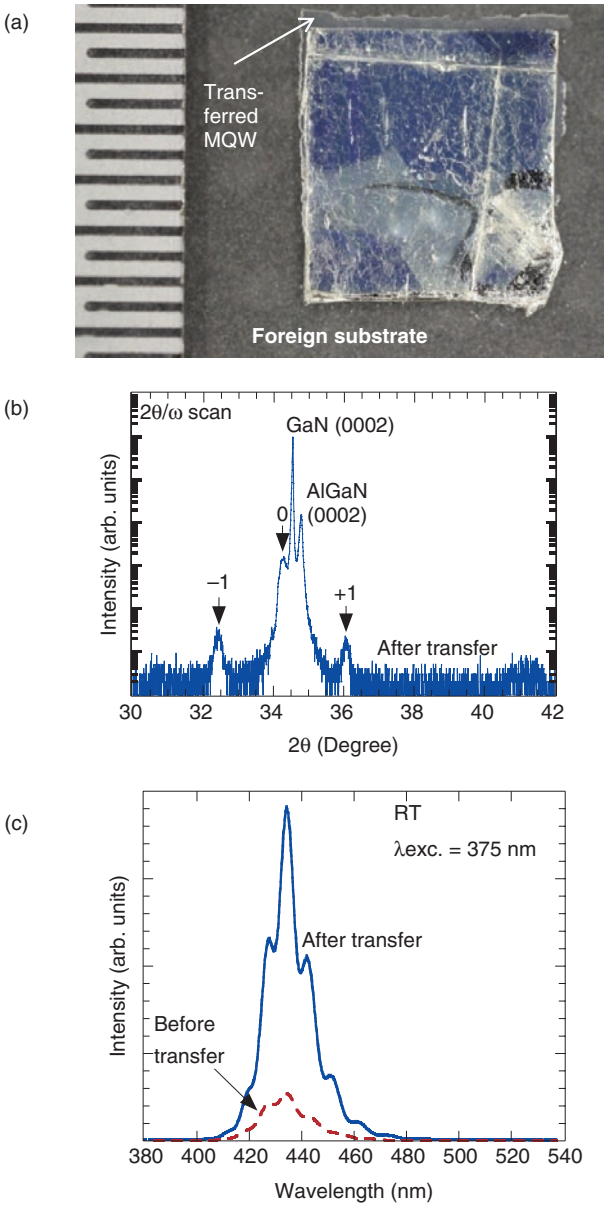

Fig. 3. Structural and optical properties of MQW structure after transfer. (a) Photograph of transferred MQW structure, (b) XRD pattern for transferred MQW, and (c) PL spectra at room temperature for the MQW before and after transfer.

AlGaN layer, the GaN layer, the ten-period InGaN/GaN MQW structure, and the GaN cap layer, was successfully transferred, and the host sapphire substrate was mechanically released. It also supports the scenario that the separation occurs in the h-BN release layer, as shown in Fig. 2(c). The intensities of the satellite peaks up to the first order after the transfer are almost the same as those before the release, indicating that the MQW structure retains its original crystal quality.

3.3 XPS measurement results

We then performed X-ray photoelectron spectroscopy (XPS) measurements of the surfaces of the transferred film and the counter-surface of the sapphire substrate after the mechanical release to verify that the separation occurred in the h-BN. The B signal was obtained for both surfaces; the position of the B 1-s XPS peak for the transferred surface was the same as that for the counter-surface of the sapphire substrate, which indicates that the separation of the film actually took place at the h-BN release layer.

3.4 PL measurement results

To check the optical properties of the InGaN/GaN MQW after the transfer, we carried out room-temperature photoluminescence (PL) measurements on the MQW before and after the transfer. An InGaN-based semiconductor laser diode with an emission wavelength of 375 nm was used as the excitation source. The PL spectra from the MQW before and after the transfer are shown in **Fig. 3(c)**. Both spectra show strong luminescence at almost the same peak wavelength of 434 nm. However, the intensity after the transfer is stronger than that before it because the indium sheet has high reflectivity in the visible wavelength region. We can also observe fringes in the PL spectrum after the transfer, suggesting that the surface of the transferred film is considerably flat. Indeed, atomic force microscopy images of the surface of the transferred films indicate that the surface is flat and has a root mean square roughness of 0.95 nm, which is consistent with the fringes in the PL spectrum in Fig. 3(c).

3.5 EL results

Next, we describe the electroluminescence (EL) emitted from the transferred LED at room temperature. For comparison, we grew the LED structures on a typical LT-AlN buffer layer on a c-plane sapphire substrate and fabricated a conventional MQW LED without using a lift-off process. The LED structures consisted of a Si-doped AlGaN layer, Si-doped GaN layer, InGaN/GaN MQW structure, and Mg-doped GaN layer. The electron and hole concentrations in the Si-doped and Mg-doped GaN layers were 2×10^{18} and 3×10^{17}cm^{-3}, respectively. The EL spectra of the transferred LED and conventional LED for currents of 10, 30, and 50 mA are shown in **Figs. 4(a)** and **(b)**. The EL intensities of the transferred MQW LED are comparable to or higher than those of the conventional LED grown on the LT-AlN buffer layer because of reflection from the back-side contact indium. Full width at half-maximum (FWHM) values of the EL of the conventional and transferred LEDs are almost the same for each current level. The comparable EL intensities and nearly the same FWHM values in Figs. 4(a) and (b) indicate that the MQW retained its original quality after the transfer. We also fabricated a vertical-type transferred LED **(Fig. 4(c))**, which can be achieved only when the LED is released from the host substrate. After the LED structure had been released, we deposited Al/Au electrodes on the back side of the LED and mounted it onto the indium sheet. An optical image of the EL from the vertical-type LED is shown in **Fig. 4(d)**. We can clearly observe blue light emission from the vertical-type LED at room temperature.

4. Prototype fabrication

We used this mechanical transfer technique to fabricate a battery-powered LED prototype, in which the released LED was sandwiched between two laminates. The LED prototype emits violet-blue EL at room temperature. In addition, we released an InGaN/GaN LED from a sapphire substrate and transferred it to a piece of commercially available adhesive tape using MeTRe [11].

The MeTRe method has several advantages compared with conventional techniques. First, this approach requires no additional equipment and no chemical etchant. Second, the process is simple and can be completed within several seconds because the process harnesses the van der Waals forces of the h-BN to release the host sapphire substrate. Finally, the separated surface after the release is essentially flat because the separation tales place in the h-BN release layer. Accordingly, MeTRe is promising for reducing the cost of the release and transfer process.

5. Conclusion

We developed the MeTRe process for releasing

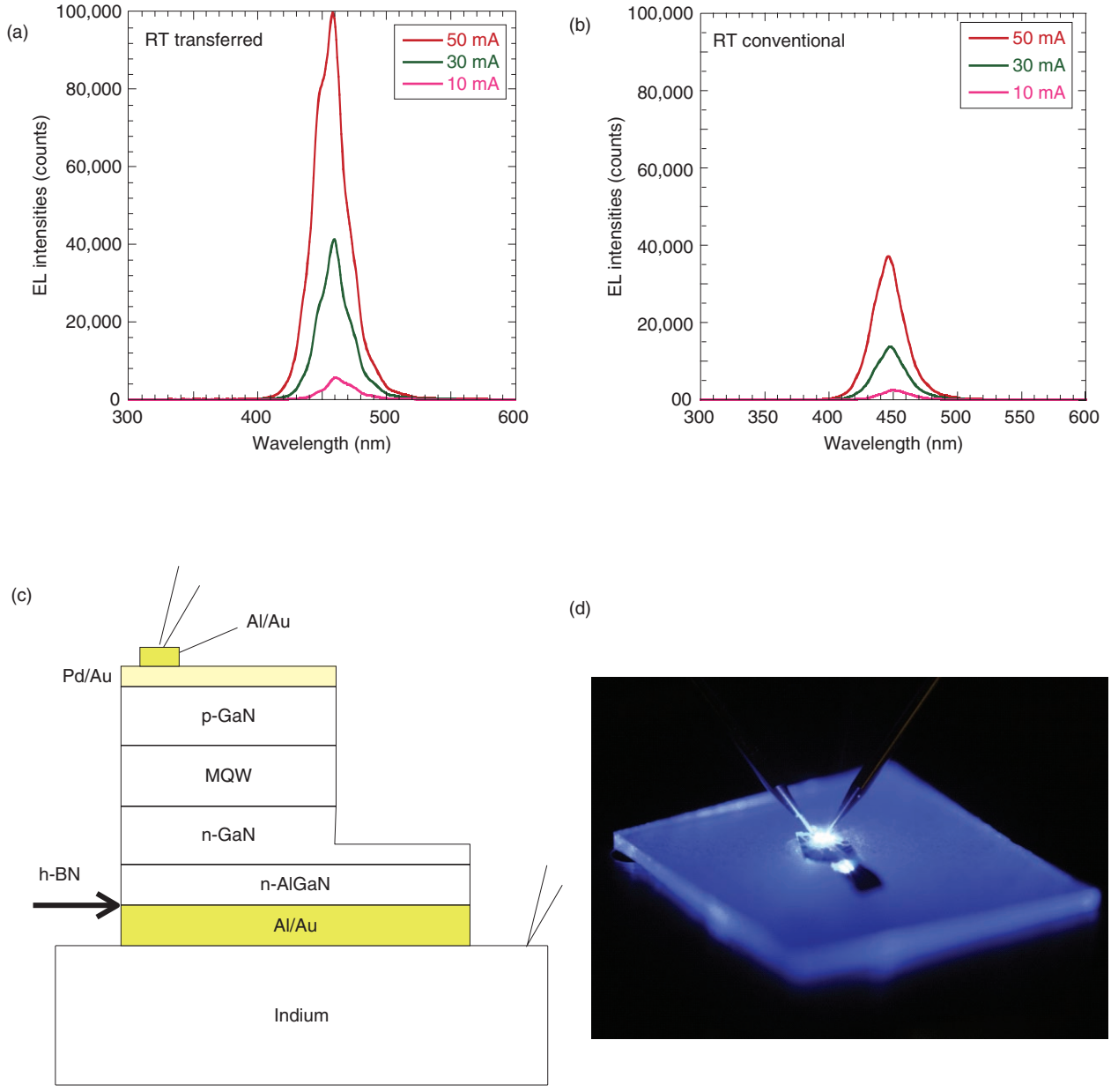

Fig. 4. EL of transferred and conventional MQW LEDs at RT. (a) EL spectra of transferred LED, (b) EL spectra of conventional LED, (c) schematic of vertical-type transferred LED, and (d) optical image of blue-light EL from transferred vertical-type LED.

GaN-based device structures from the host sapphire substrate and transferring them to foreign substrates. The mechanical transfer has been successfully used for AlGaN/GaN and InGaN/GaN MQW structures ranging in area from 25 mm^2 to 4 cm^2. We demonstrated that the intensities and FWHM of the transferred LED are comparable to those of a conventional LED, which confirms that the original device qualities are preserved even after the transfer using the MeTRe method. The MeTRe process will open up avenues of fabricating novel devices such as very thin LEDs, transparent solar cells sensitive only to ultraviolet light, and highly functional hybrid CMOS devices.

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Standardization Progress in Software Defined Networking/OpenFlow

Yoshihiro Nakajima

Abstract

The concept of Software Defined Networking (SDN) has attracted attention recently from network carriers and service providers because of its potential to provide flexible/dynamic control and programmability in network topology and packet forwarding/processing functions. In this article, we briefly describe SDN and OpenFlow and discuss their standardization trends.

1. Overview of Software Defined Networking/OpenFlow network

The use of server virtualization technologies and cloud computing is increasing substantially, and it is therefore more important than ever to ensure that network infrastructures provide high flexiblity, adaptability, and scalability from the management and provisioning point of view. Software Defined Networking (SDN) is an architecture that has been developed to achieve this [1]. In SDN, the control plane and data plane are decoupled from the existing network node that they are tightly coupled to. SDN provides a centralized operation that includes network topology management, status tracking, and other advanced controls.

An overview of a basic SDN architecture is shown in **Fig. 1**. Resources of network elements in the infrastructure layer are logically abstracted to improve functionality and performance and then provided to the components in the upper layer. The control layer analyzes the network-related control including packet routing and forwarding and assigns the control of data planes in the infrastructure layer in accordance with a request from the upper software layer, for example, the network management system (NMS).

OpenFlow is an important technology used to realize SDN. It is a layer-2 control protocol between the control plane and the data plane. An overview of OpenFlow is shown in **Fig. 2**. The items that differ between the conventional network nodes and OpenFlow nodes are also indicated in Fig. 2.

An OpenFlow controller uses a rule set of the flow header pattern for the traffic packet data plane to control packet forwarding in the data plane of an OpenFlow switch. The OpenFlow controller centrally manages how packet forwarding in the data plane of the OpenFlow switch will be handled by issuing packet forwarding/processing rules for the data plane. This architecture provides users with high programmability and configuration capabilities; therefore, fine-grained per-flow traffic control can be achieved in the OpenFlow network, where it is difficult to achieve with existing network equipment.

In this article, we describe the organization that facilitates the standardization of SDN/OpenFlow. In addition, we explain the standardization of OpenFlow, one of the most important protocols in SDN, and the future direction of these standardizations.

2. SDN/OpenFlow standardization organization: OpenFlow Networking Foundation

The OpenFlow Switching Consortium was established in 2008. The purpose of the consortium is to popularize OpenFlow networking and maintain the OpenFlow Switch Specification. Discussions on OpenFlow standardization were carried out by this consortium. OpenFlow version 1.0 and version 1.1 were respectively published in January 2010 and February 2011.

The Open Networking Foundation (ONF) [2] was established in March 2011 in order to broaden the concept of OpenFlow and to promote the

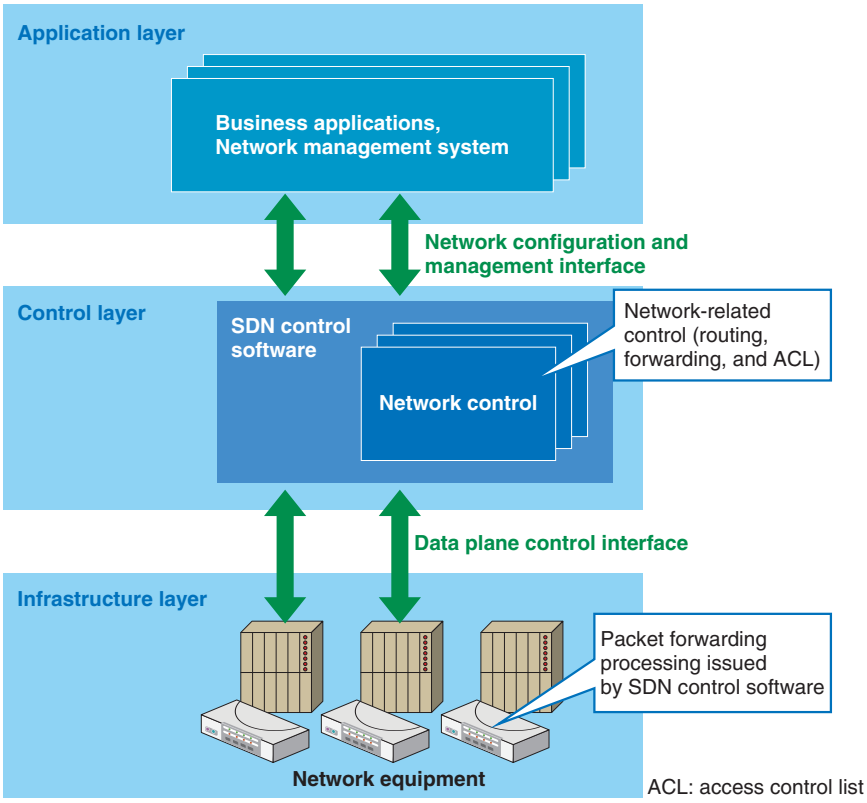

Fig. 1. Overview of SDN architecture.

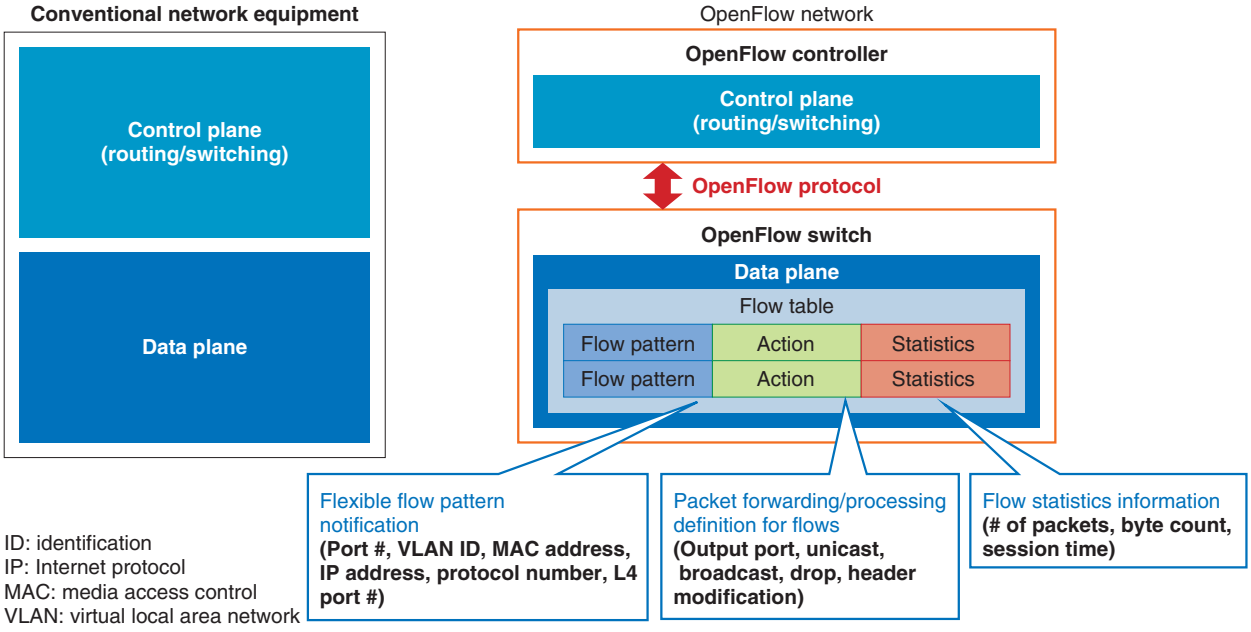

Fig. 2. Overview of OpenFlow.

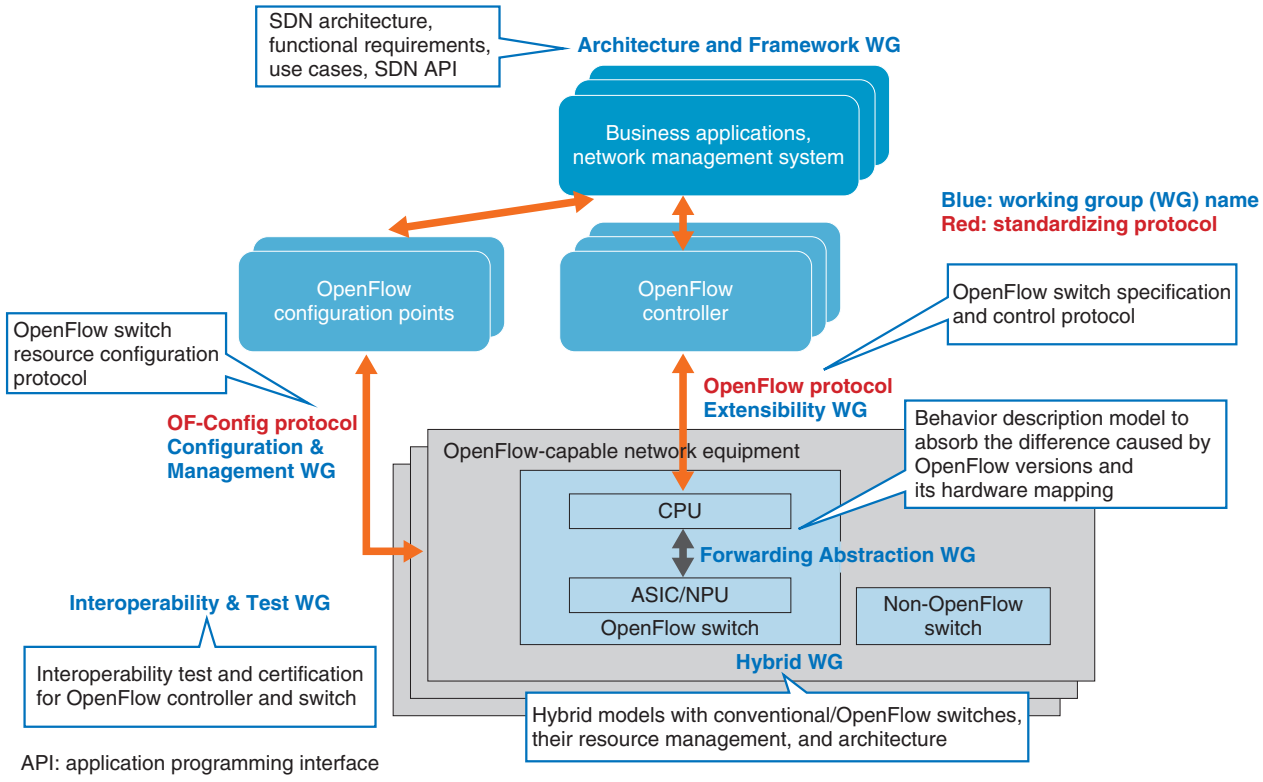

Fig. 3. ONF working groups and standardization areas.

commercialization of SDN. Activities related to the standardization process of SDN and OpenFlow specifications are now overseen by the ONF.

The ONF has formed working groups that conduct the technical standardization tasks of SDN/OpenFlow. These groups hold technical discussions, conduct compatibility test studies, and prepare charter drafts or standardization drafts for ONF board members. When a draft is approved by the ONF board members, an ONF standardized specification is issued. Discussion areas, names of working groups, and standardized protocols and technology points are shown in **Fig. 3**.

The ONF board members consist of directors of major global carrier operators including NTT, directors of major global service providers, and academic researchers. More than 70 companies, including carrier operators, software vendors, switch chip vendors, network equipment vendors, and system virtualization vendors, have joined ONF.

The OF-Config protocol has also been standardized. This protocol makes it possible to configure OpenFlow switch resources to connect to the OpenFlow controllers. Version 1.0 was published in January 2012, and version 1.1 was developed in accordance with OpenFlow 1.3.0.

3. Standardization progress of OpenFlow

The standardization of OpenFlow has been in progress since 2008. The latest OpenFlow version 1.3.0 was published in February 2012. Here, we describe the major updates and changes of each OpenFlow version.

- OpenFlow 1.0
  OpenFlow supports network protocols (e.g., Ethernet, VLAN (virtual local area network), IPv4 (Internet protocol version 4), TCP (transmission control protocol), UDP (user datagram protocol)) for campus networks and data center networks.
- OpenFlow 1.1
  Several functions in OpenFlow switches were extended to meet the requirements for wide area networks. OpenFlow supports network protocols such as MPLS (multiprotocol label switching) and the Q-in-Q extention of VLAN; these focus on inter-datacenter networks and carrier net-

works. A multiple flow table mechanism was introduced to enable packet pipeline processing in order to reduce the number of flow rules.

- OpenFlow 1.2
  Openflow added support for the IPv6 protocol in the data plane as well as for the network protocols that were supported in earlier versions of OpenFlow. An OpenFlow extensible match notification based on type-length-value (TLV) was introduced in order to achieve flexibility in protocol message parameters between the controller and switches for newly emerging protocols. A multi-controller mechanism was added to allow switches for controller failover.
- OpenFlow 1.3
  Openflow supports the operation of the control plane in IPv6 environments. Tunneling protocols, which are often used in intra-datacenter networks and virtual private networks, and provider backbone bridging (PBB) are also supported. An OpenFlow switch that adds logical port capability for link aggregation and flow control functionality for higher quality of service (QoS) to enable per-flow bandwidth control have been introduced. Furthermore, in order to support multiple OpenFlow controllers, per-flow-based traffic measurement and per-connection-based event filtering functionality have been implemented.

ONF introduced OpenFlow version 1.3.0 to provide stable specifications for network equipment vendors and software vendors in order to prevent divergence between the progress of OpenFlow specifications and the implementation of OpenFlow-enabled switches and controllers. Switch chip vendors and software vendors have proceeded with the development of OpenFlow products using OpenFlow version 1.3.0 as a target.

4. Future direction

ONF created a working group called "Architecture and Framework WG" in order to accelerate the discussions of the SDN framework and architecture. This working group is conducting discussions on the scope and standardization of SDN, SDN use cases, northbound/southbound application programming interfaces, and data models. It is also discussing SDN adaptation to transport networks, and the next generation of OpenFlow forwarding plane modeling.

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Case Study of Noise Faults Originating in Metallic Leased Lines and Countermeasure

Abstract

In this article, we introduce failure cases and a failure countermeasure for metallic leased lines. This is the fifteenth in a bimonthly series on the theme of practical field information on telecommunication technologies. This month's contribution is from the Network Service Engineering Group, Technical Assistance and Support Center, Maintenance and Service Operations Department, Network Business Headquarters, NTT EAST.

1. Introduction

The communications network is becoming increasingly faster thanks to higher capacities in the transit network and the conversion to optical fiber in the access network. In the home, meanwhile, LAN (local area network) environments using gigabit network interfaces are growing in number. This trend can also be seen in telecommunication services, where customers can get speeds of several tens of gigabits per second over wide-area Ethernet leased lines for business use [1] and a maximum speed of 200 Mbit/s on the downlink via the FLET'S HIKARI NEXT broadband service for home use [2].

In short, the NTT Group provides various high-speed communication services. What is probably not well known, however, is that it continues to provide leased-line services at the very slow speed of 50 bit/s over metallic lines. Needless to say, it is impossible to transmit large volumes of data at this speed, but these metallic leased lines are still being widely used for various applications such as remote monitoring of water-supply facilities, the transmitting/receiving of information in river management, and the transmitting of telemetric data.

The position of metallic leased lines among telecommunication services provided by NTT EAST and NTT WEST is shown in **Fig. 1**.

2. Overview of metallic leased lines

As circuits that can provide dedicated data transmission at speeds up to 50 bit/s by a direct-current (DC) method, metallic leased lines can be configured using an earth-return or metallic-return system (**Fig. 2**). The earth-return configuration enables full-duplex, bidirectional communications for transmission and reception using a single-pair cable (L1/L2: lines 1 & 2). The metallic-return configuration, on the other hand, can be used for either unidirectional or half-duplex communications. The pulses transmitted by communication devices used for metallic leased lines are of the DC type with a maximum voltage of 50 V. More technical details about analog leased lines are given on the NTT EAST website [3].

3. Metallic leased lines and noise faults

In the metallic-return system, the L1 and L2 lines are used as outward and homeward paths for the same signal, which means that the voltage induced in neighboring circuits is low.

In the earth-return system, however, different signals flow through L1 and L2; this results in a high induced voltage that can generate noise faults in neighboring circuits. These noise faults include mixing of noise in analog circuits and communication anomalies in metallic leased lines and in 3.4-kbit/s leased lines within the same cable.

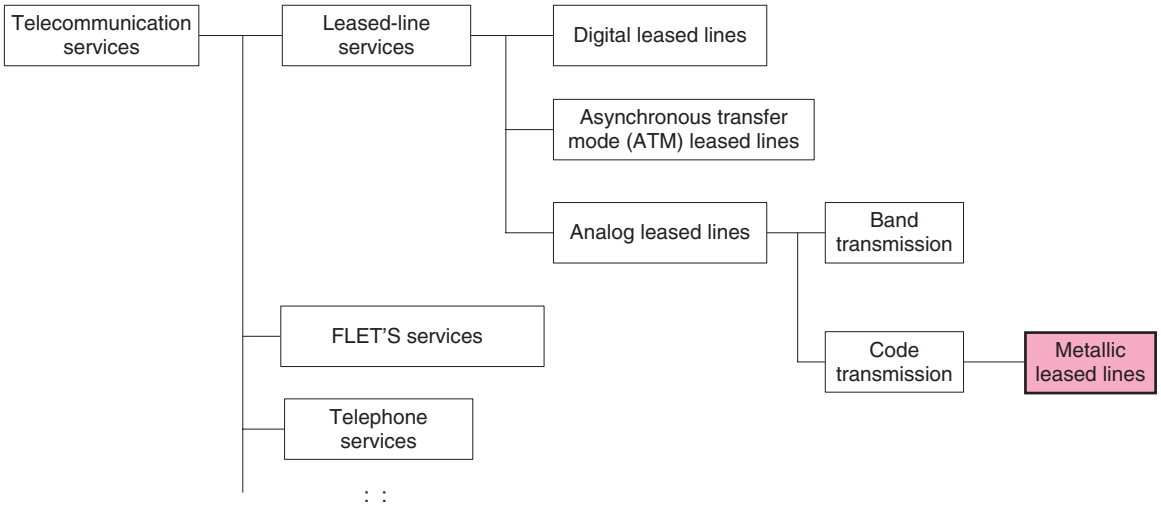


Fig. 1. Position of metallic leased lines.

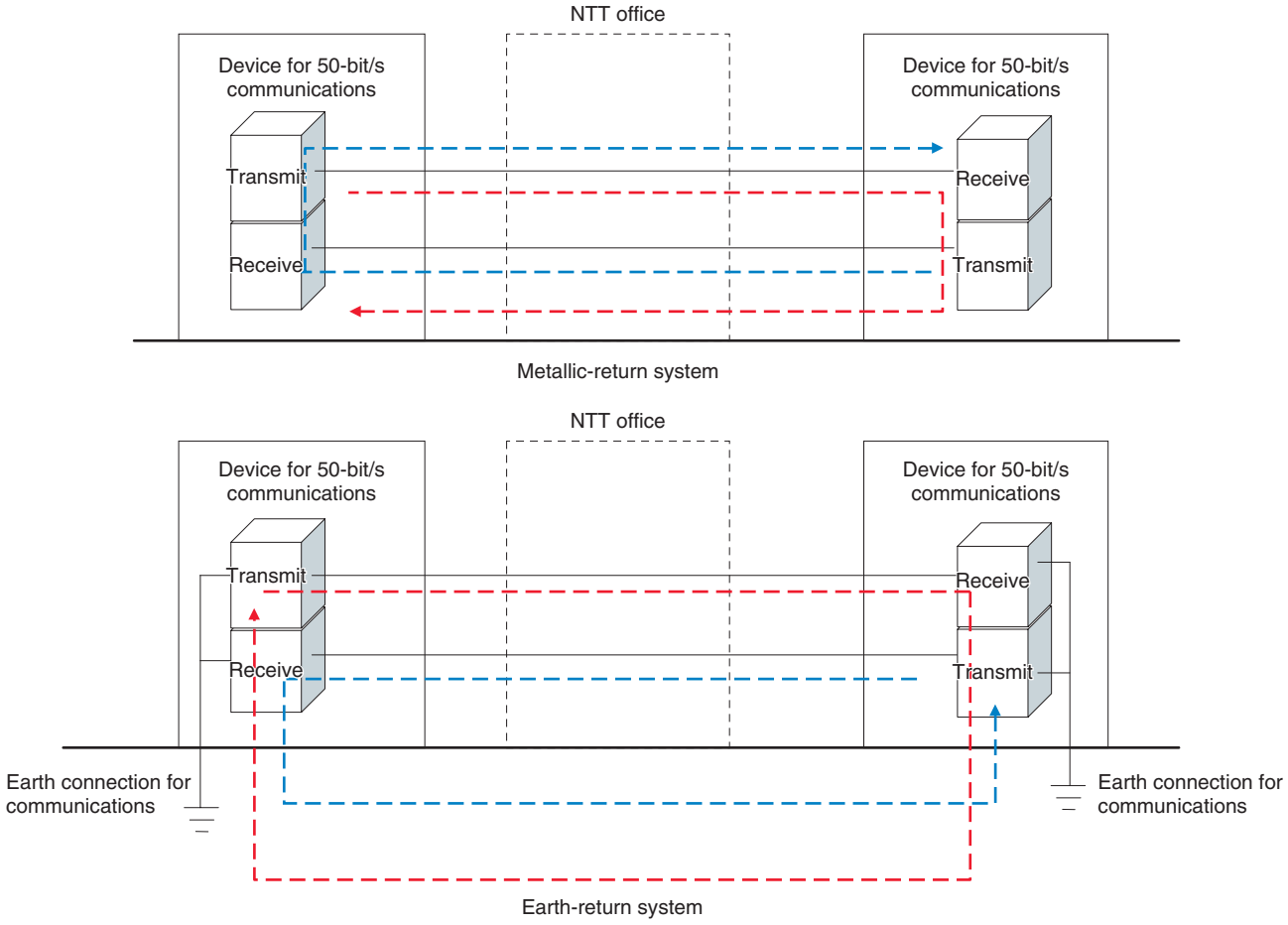
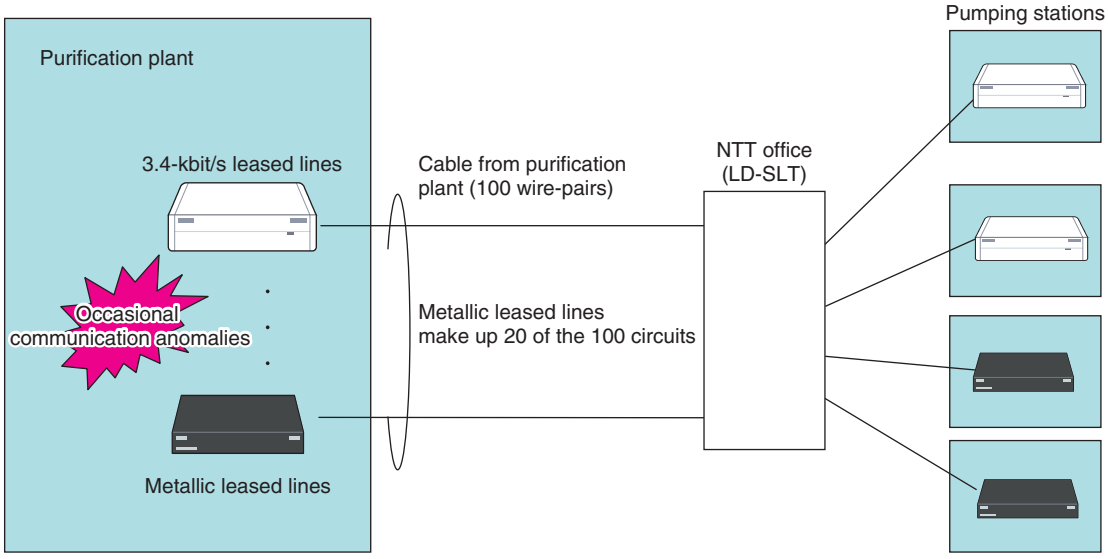


Fig. 2. Metallic-return and earth-return systems.



LD-SLT: low-speed data and analog voiceband subscriber line terminal

Fig. 3. Facility configuration.

Thus, metallic leased lines are sources of noise that can affect other circuits within the same cable and give rise to various anomalies. The next section presents a case study of noise faults caused by metallic leased lines and describes the countermeasure applied.

4. Case study of noise faults and countermeasure

4.1 Fault description and inspection results

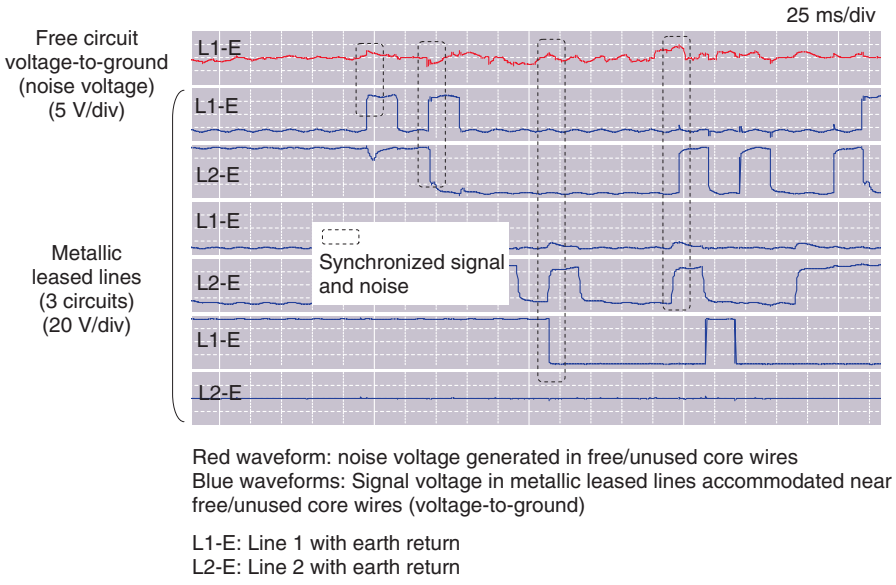
A waterworks bureau that manages communications between a purification plant and multiple pumping stations using analog leased lines (3.4-kbit/s leased lines and metallic leased lines) reported that communication anomalies were occurring from time to time in terminals on the purification-plant side. In order to switch the leased lines generating the communication anomalies to other core wires in the same cable, the fault-repair department conducted a free-wire test, but the appearance of line-testing anomalies (induced voltage detected from nearby core-free wires) indicated that many core wires could not be used. The facility configuration is shown in **Fig. 3**.

4.2 Inspection method

When the cable extending from the purification plant was checked, it was found that the cable accommodated 20 circuits of metallic leased lines using the earth-return system. Therefore, voltage-to-ground measurements of metallic leased lines and free core wires were performed within that cable to see whether noise from metallic leased lines was being mixed into other circuits. The measurement results are shown in **Fig. 4**.

These results revealed that noise constantly fluctuating in the peak-to-peak voltage range up to 10 Vpp was being mixed into free core wires. This noise was thought to be causing the line-testing anomalies discovered by the fault-repair department. It was therefore inferred that noise was being induced from the 20 metallic-leased-line circuits in the same cable. In particular, the sections in Fig. 4 marked by broken lines indicate points in these waveforms where noise was thought to be synchronized with signals in the metallic leased lines.

The cause-and-effect relationship between induced noise and signals in metallic leased lines is examined in detail in **Fig. 5**. The green and red waveforms indicate signals in metallic leased lines, and the blue waveform indicates the line voltage in the earpiece of a telephone connected to an analog circuit within the same cable. At this time, noise (sounding like "*bootz, bootz*") could be heard from the earpiece. These waveforms showed that noise in free core wires was synchronized with the rise and fall of signal voltage in metallic leased lines.



Red waveform: noise voltage generated in free/unused core wires
Blue waveforms: Signal voltage in metallic leased lines accommodated near free/unused core wires (voltage-to-ground)

L1-E: Line 1 with earth return
L2-E: Line 2 with earth return

Fig. 4. Noise in metallic leased lines and free core wires.

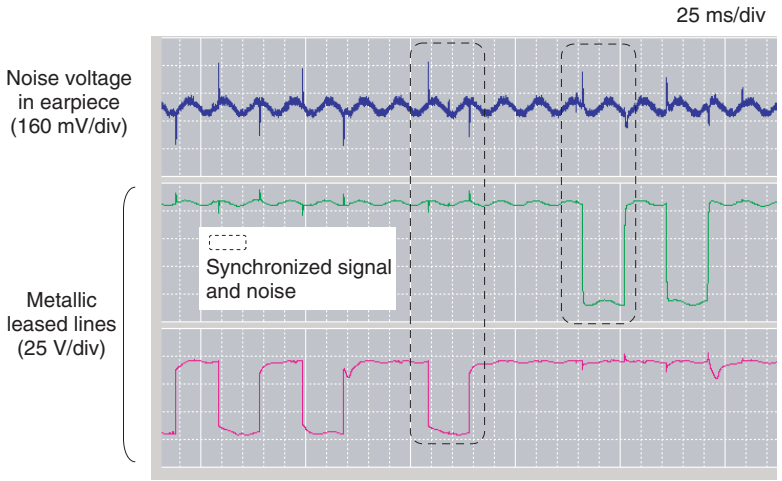


Fig. 5. Noise details.

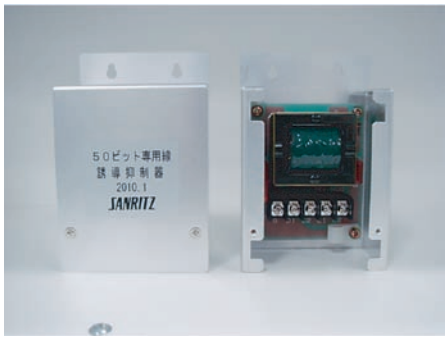


Photo 1. Appearance of induction suppressor for metallic leased lines.

4.3 Cause of fault

The results of the inspection described above led to the conclusion that the reported communication anomalies were caused by noise originating in metallic leased lines. This noise became mixed into other circuits within the same cable, resulting in communication anomalies in the 3.4-kbit/s leased lines and metallic leased lines and in line-testing anomalies in free circuits.

4.4 Countermeasure and results

Noise filters commonly used as a countermeasure to noise mixing are not effective for noise originating

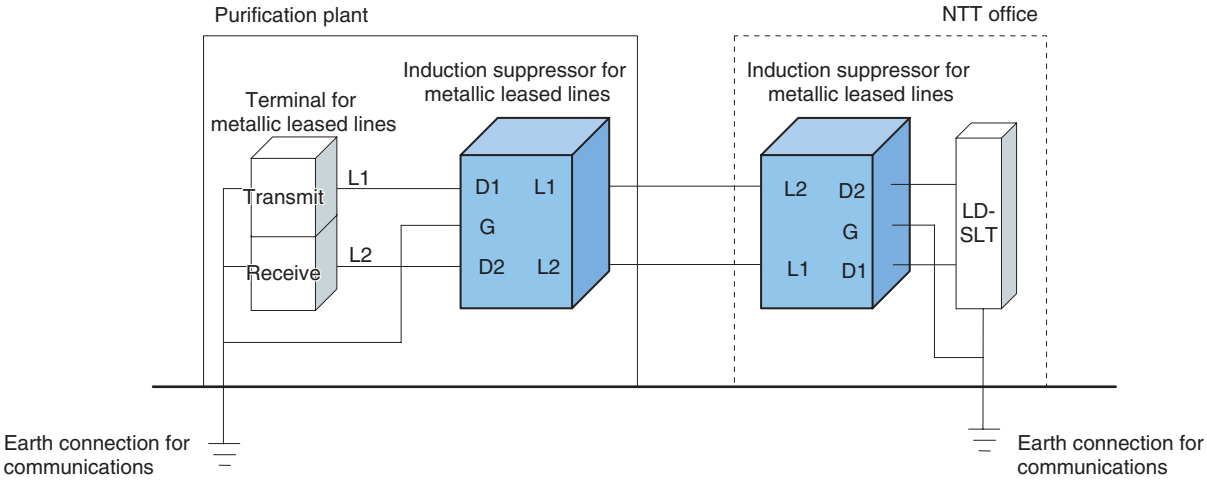


Fig. 6. Application of countermeasure device.

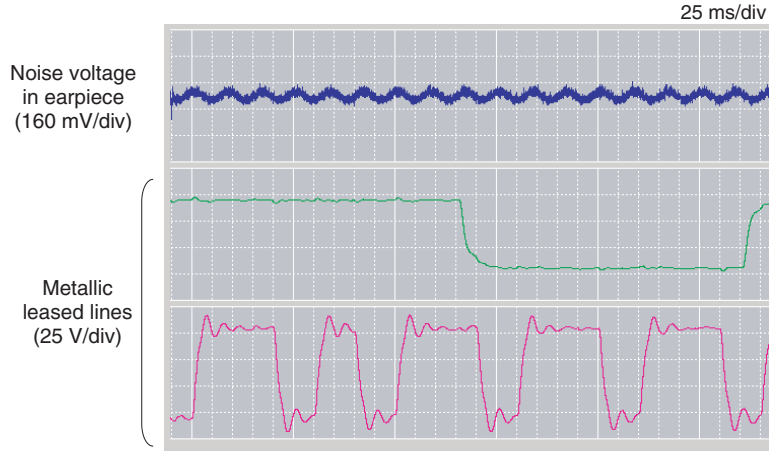


Fig. 7. Measurement results after application of countermeasure.

in metallic leased lines. This noise can, however, be effectively controlled by applying the induction suppressor shown in **Photo 1** to metallic leased lines. This device suppresses induction in other circuits by smoothing out sharp changes in the signal waveform of a metallic leased line.

The method of applying the suppressor in this case study is shown in **Fig. 6**. There was already a suppressor between the terminal and the NTT office. In this case study, additional suppressors were installed at two locations (purification plant and NTT office), since bidirectional communications were being carried out. The G pin on each induction suppressor was connected to the earth for communication purposes.

The signal waveforms after this countermeasure was applied to the metallic leased lines and the results of measuring noise at the telephone earpiece on an analog circuit are shown in **Fig. 7**. The rise and fall of signals in the metallic leased lines have been smoothed out, thereby eliminating sharp changes in those signals. As a result, no noise was observed mixing into the analog circuits.

5. Conclusion

This article introduced a case study of a noise fault in metallic leased lines and a countermeasure applied to correct it. NTT EAST and NTT WEST must

continue to maintain existing metallic leased lines despite the current expansion of high-speed broadband services. The Technical Assistance and Support Center will continue to provide support for dealing with faults unique to metallic leased lines.

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External Awards

Best Paper Award of IEEE CPMT Symposium Japan 2012

Winners: Shoichi Oshima, Kenichi Matsunaga, Hiroki Morimura, and Mitsuru Harada, NTT Microsystem Integration Laboratories
Date: December 12, 2012
Organization: IEEE Components, Packaging and Manufacturing Technology Society

For "3D integration techniques using stacked PCBs and small dipole antenna for wireless sensor nodes".

We developed ultra-small wireless sensor nodes (WSNs) that contain an energy harvester. The small WSNs can be mounted on any kind of object without affecting their volume. The use of the energy harvester means that there are no concerns about battery life. We applied two strategies to reduce the total volume of the WSNs: compact integration and device size reduction. The former involves stacking small printed circuit boards three dimensionally. The latter involves using a small electrical antenna and ultralow power wireless IC (integrated circuit) to reduce the size of the energy harvester. The fabricated 1-cm^3 and 5-mm^3 nodes can transmit ID signals using solar energy.

Published as: S. Oshima, K. Matsunaga, H. Morimura, and M. Harada, "3D integration techniques using stacked PCBs and small dipole antenna for wireless sensor nodes," Proc. of IEEE CPMT Symposium Japan 2012, Kyoto, Japan.