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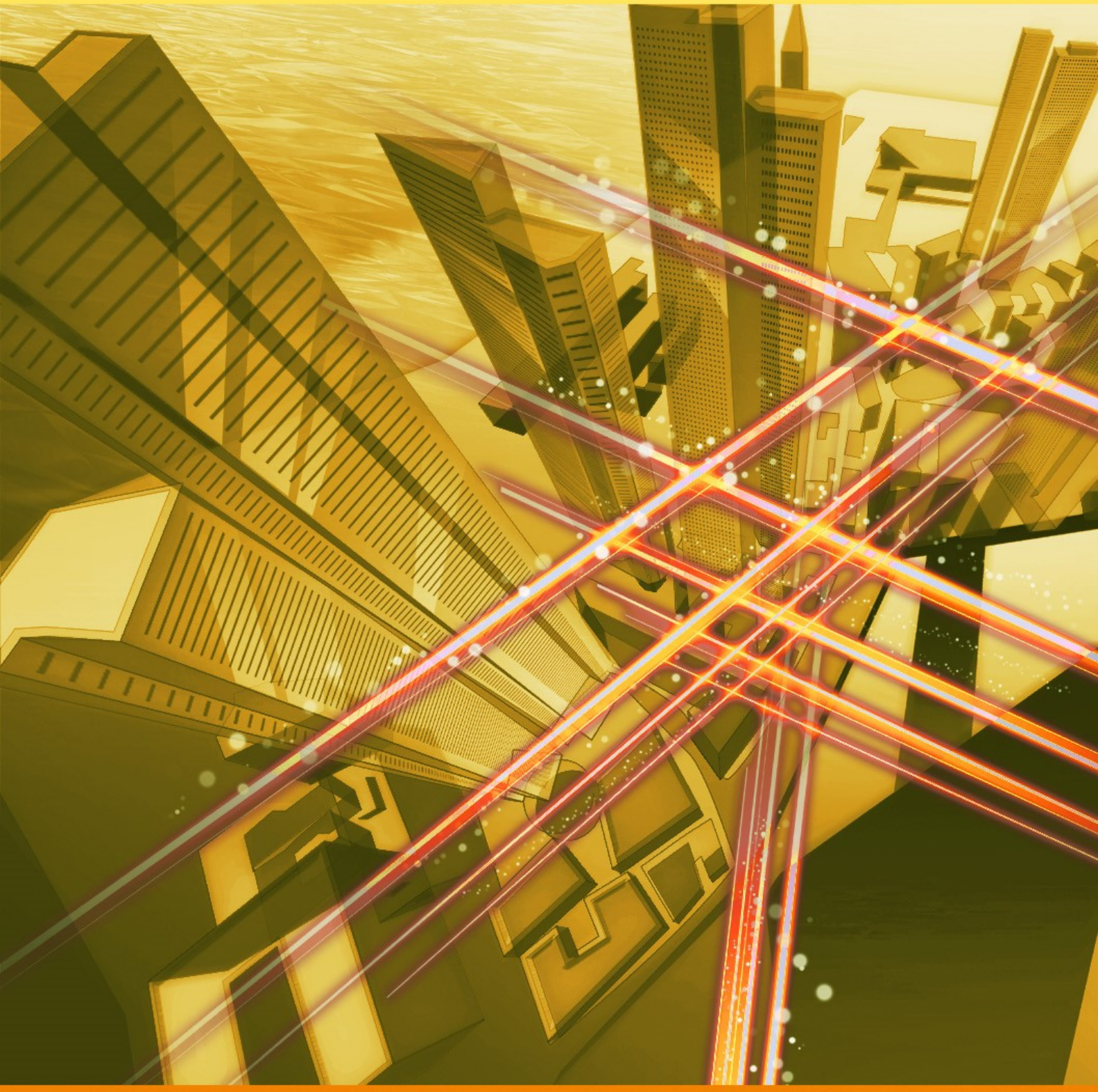

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Respect Each Other and Increase Value—Solving Social Problems by Combining World-class Strengths

Masaaki Moribayashi
Senior Executive Vice President, NTT Ltd.

Overview

As a world-leading global technology services provider, NTT Ltd., which is headquartered in London, UK, employs approximately 40,000 people in more than 70 countries and territories. While the global economy is being affected by the novel-coronavirus pandemic, the company is using technology to make a positive impact on business and society. Since the establishment of NTT Ltd. in July 2019, the company has been recognized for its contributions by, for example, being named as a leader in IDC MarketScape: Asia/Pacific Managed Security Services Vendor Assessment in March 2020 and receiving two Cisco® Partner Summit Global Awards in November 2019. We asked its senior executive vice president, Masaaki Moribayashi, about the company's business strategy and workplace culture that emphasizes diversity.

Keywords: ICT, remote, diversity

Employees and companies grow by combining strengths

—One year has passed since NTT Ltd. was established, and the novel-coronavirus pandemic has created a difficult situation. What is the current situation like in the UK?

The UK has been seriously affected by the novel-coronavirus pandemic, as in other countries. Basically, I work from home, and on a busy day, I participate in ten or so online meetings from the early morning. (This interview was conducted on July 20, 2020.) Recently, pubs and restaurants in the UK have finally begun to reopen, and the bustle of daily life is gradually returning; however, as is the case in Japan, the number of people being infected by the novel coronavirus has started to increase again, so the future is still unknown.

Although one year has passed since the company was founded, owing to various changes that have taken place worldwide, such as the novel-coronavirus pandemic, I feel that the founding of the company was a long time ago. NTT Ltd. was established by integrating 31 companies, including Dimension Data, NTT Communications' global business units, and NTT Security. The process of integrating companies involves integrating not only work but also the corporate cultures of each company. It is natural that differences exist between employees and the work they do. We strive to understand each other, but I must admit that there were many things that we didn't realize when we were working at different companies. Although it was difficult to integrate companies even within the NTT Group, I have the feeling that they now have been successfully integrated.

The integrated companies had been operating as brother and sister companies in the NTT Group. In other words, multiple companies were pursuing their own profits while expanding globally in a manner that was inefficient for the Group as a whole. To eliminate this inefficiency, integrated as NTT Ltd. and headquartered in the UK, we were able to clearly show the direction of business inside and outside the company as a unified "One NTT" brand. We have also been able to show our enthusiasm for global expansion.

At NTT Ltd., we will provide services that take advantage of NTT's strengths. I believe that one of our strengths is being able to provide a full stack of services across all layers ranging from infrastructure to applications. We are one of the world's top three datacenter providers, expanding our network solutions globally, and providing various services such as cloud and managed services. We are unique in the world in that we have such diverse service portfolios. Therefore, we are working on businesses that capitalize on this uniqueness.

We are receiving global attention and the number of proposals for partnerships and alliances has increased, reaffirming that forming partnerships and alliances are important to us. The most-important point regarding forming partnerships is that both sides receive benefits, and our alliance with Microsoft is a good example of this. Since one-sided relations do not last long, we will emphasize mutual respect and mutual enhancement of value. We think of our partnership with Microsoft in exactly this way. Since we receive many partnership proposals from global companies such as Cisco (which is closely related to the integrated Dimension Data), I feel that NTT Ltd. is highly evaluated by the industry.

—It seems that various strengths inside and outside the company are joining. Could you tell us more about NTT Ltd.'s business direction and business strategy?

Regarding our business direction, we continue to focus on providing high-value services—that is, solutions that meet customer requests and other high-value-added services—as one of the major pillars of our business. For that purpose, in addition to partnering with global companies, we are strengthening our organization with emphasis on securing and developing human resources capable of proposing our strengths in an easy-to-understand manner and construction and operation of services.

In addition, our business focuses on corporate customers, and our mission is to provide high-value-added and competitive solutions to our customers. To complete that mission, we need to make the effort to go one step further by combining the strengths of companies integrated in each field. For example, we are providing a "hybrid cloud solution." When providing cloud-related solutions to our customers, we provide them with optimal solutions by combining our private cloud and public clouds (such as Microsoft Azure) with networks, security, and managed services. I think the importance of networks is increasing as the use of the cloud increases. Our strength is providing high-quality, high-value-added network solutions encompassing connections to the cloud and SaaS (software-as-a-service) as well as in-office and remote access in an end-to-end manner. We intend to bring these strengths to the forefront and improve customer satisfaction accordingly.

We are operating business globally, so it is not surprising that 98% of employees are non-Japanese. Although about 500 employees are working in Japan, most of their colleagues around the world are of various nationalities. Having employees of various backgrounds is our strength, and we place great importance on creating an environment that respects each employee and having a positive impact on all employees. As a result, NTT Ltd. has received Top Employers certifications in 31 countries in Europe and globally in 2020 from the Top Employers

Institute, for developing human resources through business at all levels.

To fully utilize our diverse human resources, it is necessary to consider various cultural backgrounds. A questionnaire is sent to employees so we can better understand them, and a message is sent from the president to all employees who are working from home. We are also working on various measures such as enabling business training online and creating many opportunities for discussions via video conferences.

We will become a stronger company with our employees respecting each other's strengths. Moreover, if we recognize and enhance the characteristics and strengths of each of the 31 companies we have integrated, I believe that philosophy will become the culture of NTT Ltd., allowing us to grow into a strong company enhancing the One NTT brand. For example, most of the high-value services I mentioned above were developed by NTT Communications, so being able to expand them is the basis for NTT Ltd. to grow into a strong company. On top of that, Dimension Data has fully used its brand power and human resources in global development centered on solutions. I expect that we will be able to take full advantage of Dimension Data's strengths in relation to disseminating information internally to all employees and promoting brand recognition externally.

Any situation can be converted into a positive one

—In your previous position at NTT Communications, you mentioned that you would like to introduce Japanese technology and services to the world. Do you have the same enthusiasm at NTT Ltd.?

Yes, I have that aspiration. However, at the present stage, it cannot be said that the technologies and successful examples cultivated at Japanese research institutes are being transmitted to the world, so I think there are many things we can do to address this situation. In other words, there is a good possibility that our ability will be recognized globally.

In addition to the items I mentioned above, some of the initiatives NTT Ltd. has undertaken thus far are unique. For example, the Tour de France bicycle race—which is sponsored by NTT Ltd.—is already using our services. In addition to those services, we hosted a "hackfest" as an initiative to provide more technologies that could be used for other events related to the Tour de France. A hackfest is a contest in which employees are invited to come up with ideas and create solutions. I participated in the contest as a judge. Through full-scale presentations using videos, etc., professional solutions that could be used immediately were lined up one after another, and those from Japan were also selected. Despite the fact that these solutions were created by connecting countries around the world online between their regular work, they were extremely high level. Although the technologies proposed at the hackfest were designed for the Tour de France, they can be applied to similar events we sponsor, such as marathons, Indy Car races, and golf tournaments. Even though these hackfests are initiatives separate from our regular duties, I'd like to continue to make use of such initiatives because they allow our employees to demonstrate their individuality.

—What should top management be like "during coronavirus" and "after coronavirus"?

My belief is to consistently think positively. For example, I'm always thinking about how to find new directions and move forward on the basis of this pandemic. It is no longer the time to work in the office the way it used to be. If so, isn't it our job to create a remote environment in which it is easy to work? How can we improve this situation that is troublesome for many people? In a sense, this is an opportunity for us to solve social issues. That is, using information and

communication technology (ICT) to create an environment where people can work with peace of mind while working at home and produce results that equal or surpass those produced at the office.

We are currently discussing this solution internally and thinking of creating and testing a new office environment (including a remote one) and providing services in line with the "new normal." To turn this idea into reality, two key points must be addressed: first, employees must be able to work in a remote environment in which they can securely access the company's systems wherever they are. Second, the company must be able to properly manage employees and their jobs.

The novel-coronavirus pandemic is a daunting situation on a global scale, but even if it weren't, businesses sometimes fail. The important point is how to change your thinking when faced with a problem; in other words, if the best solution does not go well, you should try the second best one. If you stop thinking, you will enter a negative spiral, so it is necessary to determine when to switch to the second best. For example, to help prevent the spread of the virus, it was deemed risky for many people to gather in one place, so various events were canceled. If it is risky for people to gather at physical locations, we should focus on enabling people to gather by other means and change our mindset. We can use the power of ICT to hold safe events for many people digitally and allow people to attend seminars.

Even if employees cannot go to the office, it is possible for the CEO to send a message to employees working from home. If we change our thinking in the direction of letting the general public know that these possibilities can be fully materialized through using our technology, business opportunities will surely follow. Some of our businesses will naturally lose value because of measures to prevent the spread of the virus. Even so, we mustn't be discouraged. Instead, we should switch to more valuable and growing services. However, we must do so quickly, but determining when to switch is very difficult. Some of our employees have a lingering attachment to what they have been working on, and they may expect or be convinced that "It has been successful so far, so…" or "It may come back again." However, I believe that we at top management must show them the course of action that will allow them to dispel this belief and make the switch to the new direction.

Intuition is the result of experience and training

—How did you learn how to switch directions and judge the timing of it?

I haven't learned anything in particular, but I make judgments based on the things that I have naturally learned from my experiences. I don't know if this decision-making process is correct, and I don't think I'm 100% correct all the time. Some people say that intuition is the result of experience and training, and I feel that is close to my case.

However, blindly prioritizing the use of experience will lead to failure, so I am accumulating the amount of information and experience that should be used regarding the business of the newly established NTT Ltd. One year has passed since our establishment, and I have been able to collect a lot of information, so I think that we will be able to show our main direction in near future.

In addition to ICT infrastructure services, I have been in charge of managed services since July. For envisioning the future of NTT Ltd., using the idea of one individual is not enough, I'll combine the ideas of other executives and our parent company. When I was a little younger, I imagined that I'd be able to work a little easier at my current age. Considering my current position, however, I see that my job is getting ever tougher in a way that seems like I'm doing the toughest job in my life at NTT. If I look at my present job from another perspective, however, I see that I'm doing a fulfilling and rewarding job.

—Please say a word to our young engineers.

Good things spring from various places and people regardless of the size of a company or one's position. So many useful things and services come from little ideas, and opportunities are abundant. I hope that you will demonstrate your creativity and continue to share your thoughts. Although we are a big company, we welcome proposals from ventures. You can send information by using social media, your personal connections, or business connections via online services such as LinkedIn. The NTT Group also has a venture-capital company located on the West Coast of the United States, so when the pandemic settles down, I'll be sure to pay them a visit. In Japan, we are planning contests for ventures in Asia. So far, we have been able to hold contests in Malaysia and discover excellent technologies. I'd like to take advantage of these opportunities to connect these technologies

with our business. Connection points are everywhere, and the ideas of a single engineer can change society for the better; therefore, I hope you will continue to demonstrate your creativity.

* This interview was conducted online on July 20, 2020, and the photos used were taken previously.

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Interviewee profile

■ Career highlights

Masaaki Moribayashi joined Nippon Telegraph and Telephone Public Corporation (now NTT) in 1984. He became president and managing director of NTT Europe Ltd. in 2009, senior vice president and head of Cloud Services of NTT Communications in 2016, and senior executive vice president of NTT Communications in 2018. He has been in his current position since June 2019.

Pursuing Elegance and Creating a Research-goal Umbrella

Hirokazu Kameoka
Senior Distinguished Researcher, NTT Communication Science Laboratories

Overview

According to a survey on clumsiness while speaking of about 1800 undergraduate and graduate students of Japanese universities, approximately 30% answered that they have, or have to some extent, a problem with their pronunciation in everyday conversation, and those who were aware of the difficulty in pronunciation tended to feel that they are often asked to repeat what they said [1]. Hirokazu Kameoka, a senior distinguished researcher at NTT Communication Science Laboratories, aims to eliminate various obstacles in communication by analyzing, synthesizing, and converting voices and speaking styles. We asked him about his current research and his attitude as a researcher.

Keywords: decomposition of acoustic signals, acoustic scene analysis, speech-to-speech conversion

Development of technology for understanding a situation from sounds and converting voices according to that situation

—Please tell us about the research you are currently working on.

With the aim of creating a means by which people can communicate without inconvenience in a variety of situations, I am engaged in research on technology for decomposition of acoustic signals and acoustic scene analysis as well as speech-synthesis technology focused on high quality and naturalness. It is generally not easy to decompose a mixture into its constituents, e.g., extracting certain juices from a mixture of juices. In contrast, humans have the ability to understand acoustic scenes by distinguishing between sounds and by reading various nonlinguistic information contained in people's voices such as the tone and intention of the speaker. This ability plays an important role in people's social lives, especially in communication. For research on decomposition of acoustic signals and acoustic scene analysis, my aim is to build mathematical models and algorithms for computers to perform decomposition of acoustic signals and acoustic scene analysis.

Specifically, we, at NTT Communication Science Laboratories (CS Labs), have been working on several tasks: (i) sound-source separation, which separates and extracts multiple sounds contained in a mixed sound; (ii) sound-source identification, which identifies the nature of the target sound; (iii) voice activity detection, which estimates when the target sound is being emitted, (iv) sound-source localization, which estimates where the target sound is coming from; and (v) speech enhancement, which removes reverberation and noise to emphasize a specific voice. Conventionally, these tasks have been

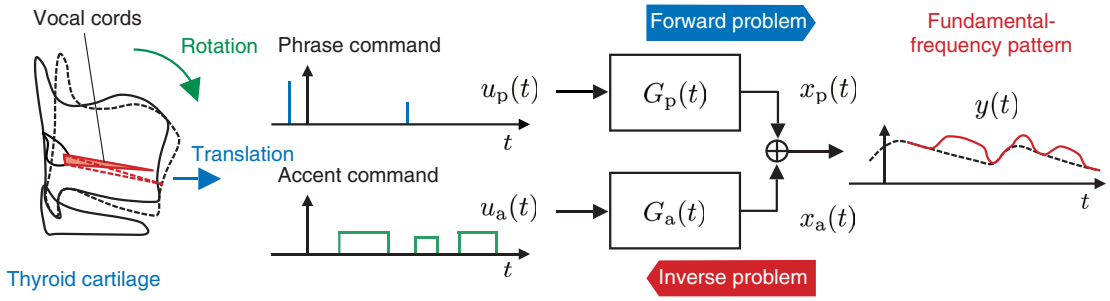

Fig. 1. Process of generating a fundamental-frequency pattern of speech and its inverse problem.

dealt with as individual research subjects. However, they are not actually independent but interdependent. For example, if sounds could be identified in advance, it would be relatively easy to separate them, and if the sounds could be separated in advance, it would be easy to localize them. In other words, the solution to one problem is a clue to solving another. From this viewpoint, instead of considering these problems as individual problems, I have approached them as joint optimization problems and devised a method of solving them collectively.

Just as multiple sounds are mixed into external sounds, various components are mixed into each voice. During conversation, we convey nonlinguistic information such as tone and intention to the other party by using the pitch of the voice together with the linguistic information corresponding to the words spoken. Speech contains elements such as phonemes related to linguistic information as well as phrase and accent components related to nonlinguistic information. The fundamental-frequency pattern, which represents the temporal change in pitch of the voice, is controlled by the thyroid cartilage that applies tension to the vocal cords, and phrase and accent components are considered associated with the translational and rotational movements of the thyroid cartilage. Correct estimation of the timing and intensity of these components can provide important physical quantities for quantifying nonlinguistic information; however, inverse estimation of these has long been a difficult problem (**Fig. 1**). In my research on decomposition and scene analysis concerning speech, I focused on the problem of decomposing the fundamental-frequency pattern into phrase and accent components and developed an efficient and accurate method for solving that problem based on a statistical signal-processing approach [2].

As an example application of this method, we implemented a demonstration system that converts standard-intonational Japanese speech into Kansai-accent intonation at events such as NTT CS Labs Open House and NTT R&D Forum. Since the content of the demonstration was familiar, it was very well received by many visitors and the press and widely covered in television programs, newspapers, and Internet articles.

This research lasted about 10 years, including the time I was in graduate school before joining the company. During that time, I was grateful to be acknowledged for many efforts. For example, I received the Signal Processing Society Young Author Best Paper Award from the Institute of Electrical and Electronics Engineers (IEEE) in 2009 and the Young Scientist's Prize of the Commendation for Science and Technology by the Minister of Education, Culture, Sports, Science and Technology in 2018. I heard that my IEEE award was the first such award to be received by a Japanese researcher. These awards improved my presence in the research field, so when I look back, I feel that they were significant events.

In addition to the research that I described above, we are working on speech synthesis with high quality and naturalness by using an approach based on deep learning. In particular, we are focusing on research on a speech-to-speech conversion technique that can flexibly convert various speech features (such as voice characteristic and rhythm) as well as fundamental-frequency patterns. There are many situations in which it is difficult to communicate smoothly. Some examples are conversations in an unfamiliar language, giving a presentation in a tense state of mind, and for people with impairment or deterioration of the vocal or hearing functions. Through research on this speech-to-speech conversion technique, we are aiming to remove such obstacles that can hinder smooth communication (**Fig. 2**).

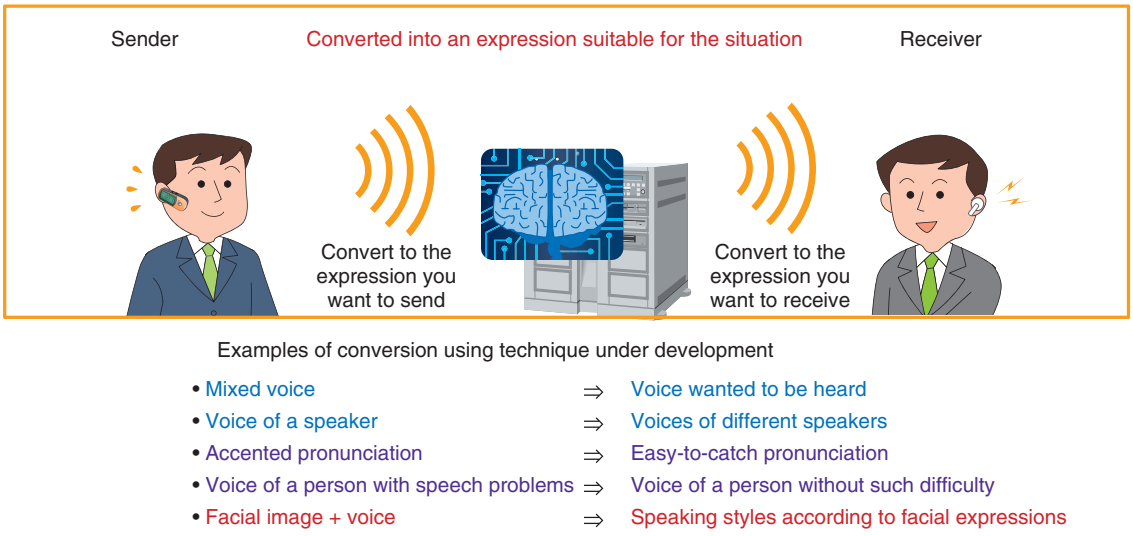

Fig. 2. Specific examples of communication-function-expansion technology.

A new perspective from the questions received at NTT CS Labs Open House

—You achieved great success. Please tell us a little more about your recent research on speech-to-speech conversion.

The fact that we decided to pursue deeper research into speech-to-speech conversion was actually triggered by an event at NTT CS Labs Open House that I mentioned earlier. Although the technique we introduced at that exhibition was used to convert an accent of the speech into another accent, one of the visitors asked the question, "Is it also possible to convert an accent of the speech uttered by a non-native speaker of English into an accent of a native speaker?" "Accent" is generally imagined as meaning a pronunciation accent of one's speech. Confusingly, in the field of speech research, it is also used as a term that means one component in the fundamental-frequency pattern, which is the meaning that we intended at that time. In fact, to convert the accent of a pronunciation in English, it is not enough to change the fundamental-frequency pattern; it is also necessary to change the *voice characteristic*, that is, the characteristic corresponding to the timbre of the voice. In other words, the technique that we introduced at that time could not handle conversion of the accent of an English pronunciation. That being said, that question got me a bit more interested in the problem of translating English-pronunciation accents. In the field of speech research, a technique called voice conversion, which converts an input voice into another person's voice, has been developed. In anticipation that this technique is probably the most relevant to the problem of translating English-pronunciation accents, I implemented and experimented with a current method of voice conversion.

However, it turned out that this method could change only the speaker identity; it could not change the speaking style such as the accent of a pronunciation. At this time, I felt that this problem was deeper and more interesting than I had imagined, so I decided to tackle the problem of voice conversion more seriously and focus on the broader problem of speech-to-speech conversion. Around that time, with the advent of deep learning (so-called artificial intelligence (AI)), I started working on speech synthesis and conversion using the deep-learning approach. In the four years that have passed since then, I have investigated various approaches in collaboration with colleagues and trainees, and we have created many high-quality and flexible speech-to-speech conversion techniques that can convert not only English-pronunciation accents but also a wider range of speech features.

—Why did you decide to work on acoustic signals and speech synthesis?

When I was a student, I played guitar in a band. If I had a favorite song, I often practiced it after listening

to the sound and wrote it down as a musical score, so-called "playing by ear." For my graduation thesis, since I wanted to work on a theme related to my interest, I decided to research an algorithm that automatically plays by ear. That decision gave me the chance to knock at the gate of a laboratory that studies sound. I knew nothing about that field of research, but I remember being excited when imagining how to use my knowledge of signal processing and statistics that I learned at university. At the time, I had a longing to sing better, but I didn't really feel confident because I didn't really like my singing voice. Therefore, besides automating playing by ear, I wondered if I could automatically convert my voice into a good singing voice. Many researchers who study speech are interested in music, and quite a few of them started their research for similar reasons. In my case too, such a simple motive has led to my current research. Looking back now, I feel that the dual motivations to automate playing by ear and improve my singing voice have something in common with my current research—which aims to support human hearing and vocalization functions.

What we can do musically is restricted by our musical skills, such as playing by ear, playing musical instruments, and singing. In the same way, in our daily communications, we face various restrictions due to physical and psychological conditions. My current interest is to remove such restrictions through the power of machine learning (AI) and signal processing and create an environment in which everyone can communicate comfortably and freely. To reach this goal, I think two technologies will be key. One is scene analysis, which captures the situation and environment in which the sender and receiver are located, and the other is media conversion, which converts the information that the sender wants to convey to the receiver into an expression suitable for the situation. I also want to explore the possibilities of new communication method that makes effective use of not only sounds but also multiple media, such as video images and text, and create the basic technology to implement them.

Expanding what you can do, what you want to do, and what is required while creating a research-goal umbrella

—Has anything changed since you became a senior distinguished researcher?

My research life has not changed much so far, but I want to focus on the following two objectives. The first is the objective that I have attempted to achieve as a researcher, that is, to expand the range of "what I can do," "what I want to do," and "what is required." The second is to create a research-goal *umbrella*. I learned the importance of having such an umbrella in the group to which I was assigned when I joined NTT. Having a clear research goal on which everyone can agree on its usefulness to society will allow researchers to focus on the difficult issues at hand and be confident in the direction they should take. Research activities are the work of steadily accumulating research results, of which each one is not necessarily a big success. Therefore, we may sometimes suddenly become anxious that what we are doing is nothing special. When I joind NTT, I was able to study with confidence under the umbrella that my senior colleagues created. This is exactly like being protected by an umbrella of a research goal. Therefore, as a senior distinguished researcher, I have become even more strongly motivated to make sure everything is crystal clear to junior researchers and that everyone involved can feel at ease and make progress without hesitation. I believe that to expand the range of "what I can do," "what I want to do," and "what is required," and create a research-goal umbrella will only be possible if I continue to improve and grow. With that in mind, I will continue to work hard and not accept things as they are.

On the contrary, I also try to keep in mind that one matter should remain unchanged. That is my research style, namely, *pursuing elegance*, which is also my policy as a researcher. This policy was formed during my university days when I was greatly influenced by the research style and thoughts of my supervisor who was a former NTT researcher. Elegance is hard to define, but it's an aesthetic sense for a skillful approach that sees the true nature of things. It may be similar to what we feel when we come across elegant problems, solutions, and proofs in mathematics. By pursuing elegance in everything we do, I think we should be able to sharpen our thoughts and climb to higher levels. In my life as a researcher, I have felt confident in my achievements, but I still feel they are not enough, so I want to continue pursuing elegance and continue writing as many papers as possible.

—Please say a few words to your junior researchers.

Although research is often difficult and emotionally demanding, I think it is most important to enjoy researching at NTT and your research. Research does

not progress when you are depressed or when your thoughts are blocked by delusions; conversely, when your spirits are high, research progresses.

Since the speed of your research will change in accordance with your feelings, it is important to keep your frame of mind stable and look forward. For example, we tend to think that we want to beat someone or show off to people around us. That thinking stems from being overly conscious of others and overwhelmed by negative emotions such as jealousy and impatience. Therefore, I think it's a good idea to focus on whether you are growing day by day without worrying about problems that are beyond your control. By looking forward to your own growth, even if you hit a brick wall, you will feel like trying harder to get over it.

You should also be careful when you get too absorbed in your research. At first glance, although it seemed that everything was going well at the time, when you look back later, you often find that your research actually had stalled. I'm prone to the same thinking, but, at such times, your perspective is usually narrowed. That is a state of pouring your heart and soul into your research while believing that what is objectively not so important is important. If you are not alert, you can fall into such a state anytime, so it is necessary to cultivate a sense of calmness that allows you to look at yourself objectively at all times as well as the ability to concentrate on what is in front of you. This means it is important to have two personalities—one that works diligently and one that is calm and objective—and consciously continue a dialogue between those two personalities.

I consider researchers to be providers of wisdom to change the world for the better. Of course, NTT researchers conduct research for NTT, but from a more macroscopic perspective, the common mission of all researchers is to make the world a better place. Although we need to be strong enough to compete with others, we must also have the integrity to be respectful of the research and contributions of others with the same mission.

—Please tell us about your future goals and prospects.

I will continue to pursue research focusing on how to facilitate human communication. Looking beyond that pursuit, we're aiming to achieve *cross-media conversion*. Audio, text, and video images are media with different characteristics. For example, audio is useful when you want to express a message quickly and convey it to another party, and text is useful when you want to quickly read the main points of the message. An advantage of video images is that they can express detailed information that cannot be expressed through audio or text alone. I believe that by taking advantage of the features of each of these media and allowing the sender and receiver to flexibly select the media to use according to the situation in which they are in, it will be possible to achieve efficient and smooth communication. To make that possibility a reality, we have to enable cross-media conversion, namely, transforming each media signal into a different media signal in a manner that retains the message or content. I think this task will be a very challenging and interesting theme.

As a researcher, I'd like to pursue beneficial research themes and elegant approaches. Each field has so-called *star* research themes. However, although that star theme is important, it might be an impregnable subject that many researchers have been tackling for years. Benchmarks, evaluation systems, and data sets have already been established for these research themes, making research and experimentation relatively easy. However, it requires fairly high degrees of specialized knowledge and skills to make a difference while many researchers compete. In contrast, it is also important to work on pioneering new themes that no one has focused on. This can add value to the field and help create a new world. However, in some cases, it is necessary to construct an evaluation system and data set from scratch, so it takes much effort to launch such research. I'd like to cultivate a high degree of expertise and flexible creativity and strive to solve various problems while striking the right balance between both types of efforts.

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■ **Interviewee profile**
Hirokazu Kameoka
Senior Distinguished Researcher, Media Information Laboratory, NTT Communication Science Laboratories.

He received a B.E., M.S., and Ph.D. from the University of Tokyo in 2002, 2004, and 2007. He is currently a senior distinguished researcher and senior research scientist with NTT Communication Science Laboratories and an adjunct associate professor with the National Institute of Informatics. From 2011 to 2016, he was an adjunct associate professor with the University of Tokyo. His research interests include audio and speech processing and machine learning. He has been an associate editor for the IEEE/ACM Transactions on Audio, Speech, and Language Processing since 2015 and a member of the IEEE Audio and Acoustic Signal Processing Technical Committee since 2017.

All-Photonics Network and Photonics-electronics Convergence Technologies as a Vision of the Future

Tetsuomi Sogawa, Masato Tomizawa, Akira Okada, and Hideki Gotoh

Abstract

This article presents the Innovative Optical and Wireless Network (IOWN) proposed by NTT and the All-Photonics Network—a key element of IOWN—as a vision of the future along with the technologies for achieving it. It also introduces photonics-electronics convergence technologies as the key to achieving an ultralow-latency and ultralow-power consumption of the All-Photonics Network and its roadmap.

Keywords: IOWN, All-Photonics Network, photonics-electronics convergence

1. What is IOWN?

NTT aims to build a prosperous society in which people recognize diverse concepts of values. Obtaining information and sensations from another person to deepen mutual understanding should contribute greatly to achieving such a new and highly diverse world. To achieve this world through research and development, there will be a need not just to obtain large amounts of information through communication infrastructures that are more massive than ever before but also to process that information on a level that includes human feelings and subjectivity.

Toward achieving this future vision, NTT has put forward the concept of the Innovative Optical and Wireless Network (IOWN) as an unprecedented communications platform. The aim is to achieve a network and information-processing platform featuring ultralarge-capacity, ultralow-latency, and ultralow-power consumption capabilities through innovative technologies centered around photonics. NTT has started to discuss with various partners toward achieving IOWN in 2030.

IOWN consists of three key elements: the All-Photonics Network (APN), which introduces photonics-based technologies throughout the network even as far as user's terminals in an end-to-end manner; Cognitive Foundation®, which centralizes management, operation, deployment, configuration, and interlinking of information and communication technology resources in different devices such as edge computers, network services, and user equipment, all from the cloud; and Digital Twin Computing as a new computing paradigm that combines many items of digital information representing the real world and simulates different forms of interaction between objects and humans in cyberspace. Each of these elements targets a different layer, but in combination, they can achieve a new generation of networks and information processing.

2. Importance of the APN

Among the above three elements, the APN is the foundation of new optical communications and information processing. As its most outstanding feature, it is aimed at achieving an information-processing infrastructure with low-power consumption and high-speed information transmission through a transition from conventional electronics to photonics (**Fig. 1**). The target power consumption is to increase power efficiency by 100 times through the introduction of the photonics-electronics convergence technologies described below. The target transmission capacity, meanwhile, is a 125-fold increase made possible by, for example, the development of multicore fiber that

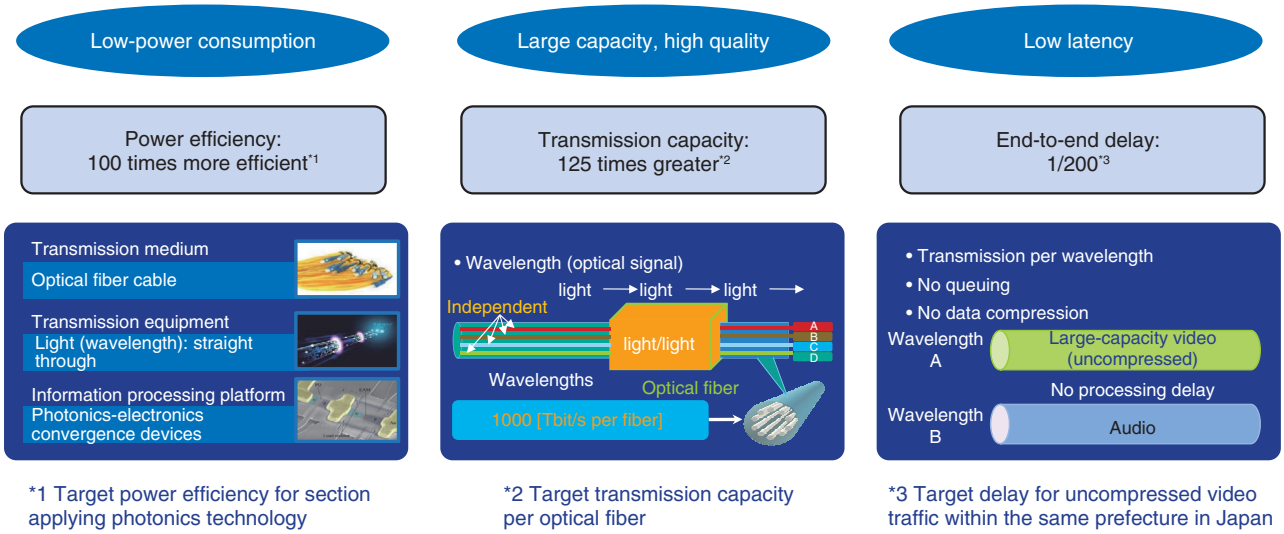

Fig. 1. APN performance targets.

accommodates many cores within a single optical fiber and the development of a coherent optical subassembly. Furthermore, the target end-to-end delay is 1/200 of the current level by, for instance, transmitting data in uncompressed form in the case of applications that cannot allow for any delay.

3. Examples of diversity and application through the APN

When the APN is achieved, we can expect various new scenarios. Due to the limited bandwidth of a current network, the amount of data in information to be transmitted has been purposely reduced using a technique such as sampling, quantization, and data compression when analog data are converted to digital data. In contrast, the dramatic leap in transmission capacity in the APN will make it possible to send and receive information with high resolution and a high sampling rate, which is faithfully closer to the original signal. Furthermore, if data that cannot be perceived by humans, such as a bee's sense of sight, dog's sense of smell, or bat's sense of hearing, are maintained and exchanged without data compression, it should be possible to greatly extend the five human senses and create a society that enhances the human capability of empathizing with others.

If different optical wavelengths were to be allocated to each different function and service in optical fiber transmission, it would be possible to transmit multiple streams of information simultaneously with low latency. For example, interactive exchanges between people with no delay could take place while transmitting high-definition images over multiple channels. As a result, applications with critical requirements for communications quality, such as remote surgery and mobility as a service, could be made practical.

4. What are photonics-electronics convergence technologies?

To successfully achieve the APN, we should introduce photonics-electronics convergence technologies, which combine electronics and photonics technologies in the signal processing section of a processor chip. This extends the role of photonics, which has conventionally been used for long-distance and medium-distance transmission such as in interconnects within datacenters.

NTT laboratories achieved a milestone in the development of photonics-electronics convergence technologies by fabricating an optoelectronic conversion device that operates on the world's smallest amount of consumed energy. This achievement was published in the British scientific journal *Nature Photonics* on April 15, 2019 [1]. Technology for integrating light with part of an electronic circuit has been investigated for over 20 years, but large device size and power consumption prevented this technology from becoming practical. The technology presented by Nozaki et al. [1] succeeded in cutting power consumption by 94% compared with current technology.

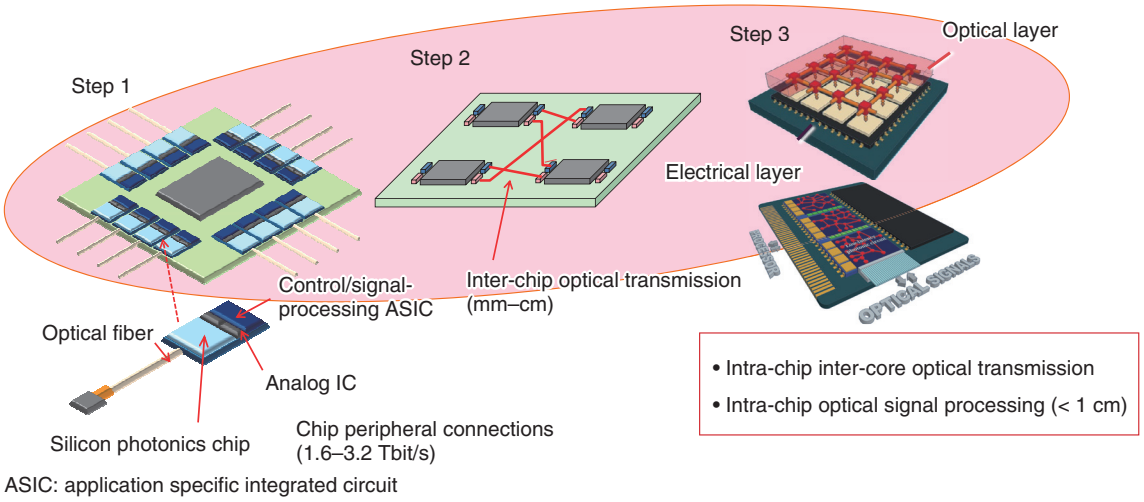

Fig. 2. Roadmap of photonics-electronics convergence technologies.

The roadmap for photonics-electronics convergence technologies is shown in **Fig. 2**. The first step will be to fabricate a structure that integrates circuits using silicon photonics with fibers and analog integrated circuits (ICs) and achieve ultrahigh-speed connections with peripheral circuits outside the chip (Step 1). The next step will be to directly interconnect chips by ultrashort optical wiring to improve information processing performance (Step 2). The last step will be to lower power consumption by interconnecting cores within a chip by optical wiring and applying optical transistors. We also aim to achieve arithmetic processing instantly only in the light propagation time of the optical circuit by using optical pass gate technology, which make maximum use of optical characteristics (Step 3).

5. Content of feature articles

The Feature Articles in this issue take up photonics-electronics convergence technologies toward the APN at the NTT Science and Core Technology Laboratory Group. They will introduce the above steps: Step 1 achieving ultrasmall optical transmit/receive circuits using silicon photonics technology [2], Step 2 targeting high-density, low-power optical interconnections [3], and Step 3 focusing on optoelectronic conversion devices and optical pass gate circuits using nanophotonics technology [4].

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Ultracompact Silicon Photonics Coherent Optical Subassembly for Ultrahigh-capacity Optical Communication

Yusuke Nasu and Shogo Yamanaka

Abstract

Toward the All-Photonics Network, which is a key element of the Innovative Optical and Wireless Network (IOWN), we at NTT Device Innovation Center are developing an ultracompact optical transceiver module as a photonics-electronics convergence device. By using silicon photonics technology and co-packaging electronic devices, we fabricated an ultracompact coherent optical module for next high-capacity optical networks.

Keywords: silicon photonics, digital coherent, coherent optical subassembly (COSA)

1. Introduction

Along with the diversification of communication services, the data traffic that should be processed by information technology (IT) systems in a network has increased dramatically, and the amount of power consumed by IT systems has increased. Therefore, NTT proposed a network concept called the Innovative Optical and Wireless Network (IOWN) to manage the ever-growing traffic and provide a communication network with even greater capacity, lower latency, lower power consumption, and flexibility.

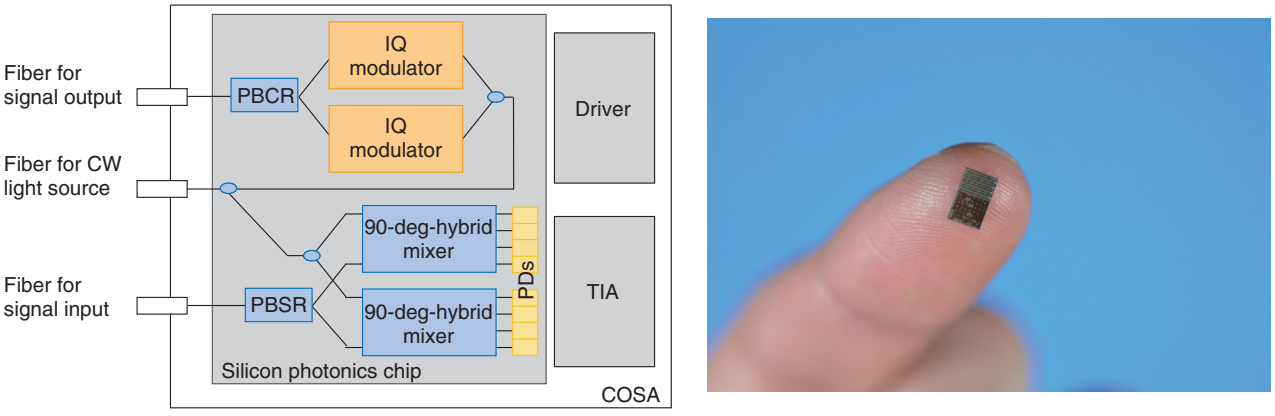
The All Photonics Network (APN), one of the key elements of IOWN, introduces photonics everywhere in a communication network. By applying photonics for shorter distance transmission than current networks, the APN is aimed at achieving low power consumption, and high-quality, large-capacity, and low-latency transmission. To adopt photonics to shorter distance transmission, it is necessary to dramatically reduce the size as well as cost of photonics devices. Photonics-electronics convergence technology [1] is a key enabler for such improvement.

At NTT Device Innovation Center, we are developing optical transceiver modules using silicon photonics technology to not only minimize optical interfaces for high-speed transmission but also to reduce power consumption. By integrating an optical circuit into a single silicon chip and co-packaging this with an analog electronic circuit, we developed an ultracompact coherent module for digital coherent transceivers. We call this module coherent optical subassembly (COSA). This integration is a photonics-electronics convergence technology and can significantly reduce the size and cost of the optical interface in a network.

2. Silicon photonics technology

Since the early 2000s, NTT Science and Core Technology Laboratory Group has been working on silicon photonics technology and is a pioneer in this field. Silicon photonics technology uses transparent silicon in the communication wavelength band (1.3 to 1.5 μm) as a platform for optical integrated circuits (ICs) by using the fabrication technology developed for large-scale integrated circuits.

Silicon photonics technology enables the mounting of not only simple optical passive elements but also



CW: continuous wave
IQ: in-phase and quadrature
PBCR: polarization beam combiner rotator
PBSR: polarization beam splitter rotator
TIA: transimpendance amplifier

Fig. 1. Conceptual diagram of COSA (a) and image of silicon photonics chip (b).

optical active components, including optical modulators and germanium photodetectors (PDs), on silicon. Optical devices in optical transceivers have traditionally been fabricated using different material systems. These conventional discrete devices are interconnected using optical fibers and spatial optics. NTT has succeeded in developing key optical devices by using silicon photonics technology and integrating them on a single silicon chip. By mounting such a silicon photonics chip together with an electronic circuit in the same package, a compact optical module for an optical transceiver can be fabricated.

3. COSA for digital coherent transmission

Digital coherent transmission can compensate for the various optical signal distortions received during optical transmission due to its powerful electrical compensation technology and has been developed for long-distance transmission from hundreds to thousands of kilometers. We are currently studying the application of such digital coherent transmission technology even for short-distance applications such as intra- and/or inter-datacenter communication where the traffic has increased remarkably during the last decade.

The Optical Internetworking Forum (OIF), which is an industrial association promoting network solutions through the creation of Implementation Agreements, defines standards for power consumption and the size of digital coherent optical transceivers. OIF has set a new standard for digital coherent optical transceivers every one to two years since 2012 and demands smaller sizes each time.

Around 2012, the standardized size of a transceiver was 12.7 × 17.8 cm, but a smaller size of 2 × 8 cm is currently required. Such a small form factor is called quad small form factor pluggable-double density. At the same time, standard transmission speed also increased from 100 to 400 Gbit/s. Expanding traffic related to datacenter networks mainly drove such demand for reducing the size and increasing bandwidth. Therefore, NTT argued that silicon photonics technology can be used for digital coherent optical transceivers [2].

A conceptual diagram of COSA is shown in **Fig. 1(a)**. A silicon photonics chip, transimpedance amplifier that converts the output current of the receiving PD into a voltage signal, and driver that drives the optical modulator are integrated in one package. In the silicon photonics chip, an in-phase and quadrature modulator and polarization beam combiner rotor is integrated on the transmitter side. On the receiver side, a polarization beam splitter, 90-degree optical mixer, and high-speed PD array are integrated. On both transmitter and receiver sides, a PD for monitoring the optical signal power of transmission and reception is also integrated. In a conventional coherent transceiver, these optical elements are separate devices using different material systems and

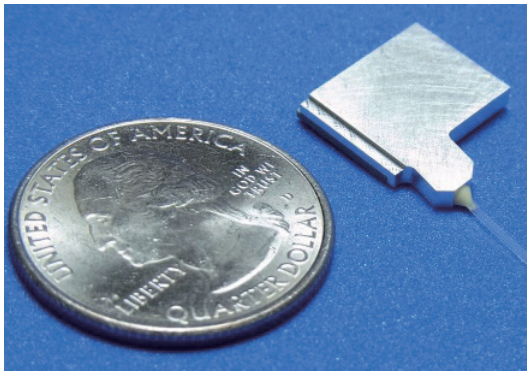


Fig. 2. Image showing size of COSA.

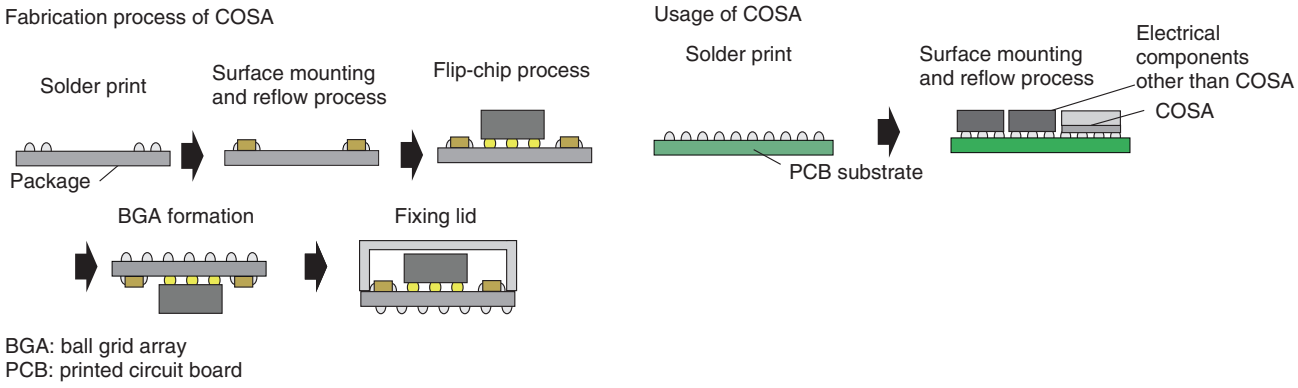
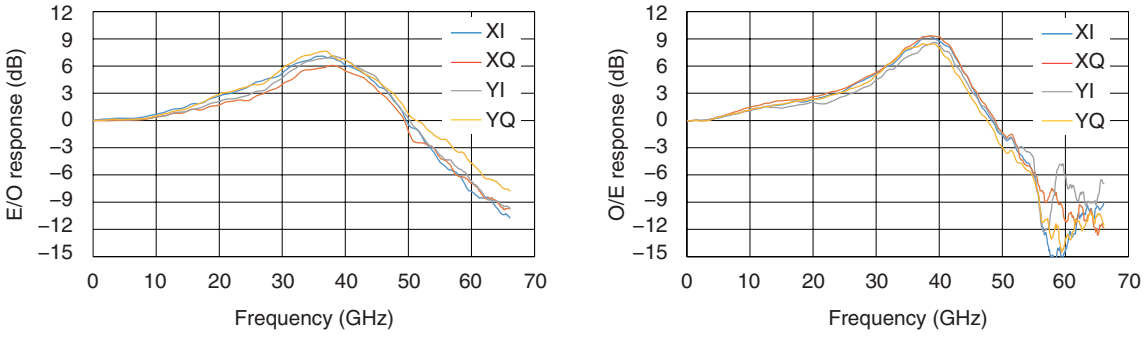


Fig. 3. Diagram of COSA assembly process.

are interconnected by optical fibers, optical lenses and so on. Therefore, there is a limit to reducing the size of the transceiver. COSA integrates these key optical devices on a single chip, so dramatic size reduction can be achieved, as shown in **Fig. 1(b)**. This chip was mounted in a package together with drivers and electronic devices as COSA for 400-Gbit/s transmission.

We also removed the temperature control units, which are often used in conventional optical components, to reduce the module size. This is the result of the temperature-independence design of the circuits in a silicon photonics chip. The humidity-tolerant design of each chip in COSA also enables us to reduce the module size because we can use a non-hermetic package, which is smaller than the conventional hermetic package. The optical coupling structure based on the directly attached fiber on the silicon edge also contributed to downsizing the device footprint and height. **Figure 2** is a photograph of COSA. COSA is currently available in a very small and thin package of 19 × 12 × 2.1 mm. Now that the miniaturization of digital coherent optical transceivers is progressing, further miniaturization is expected to accelerate by applying COSA.

Figure 3 shows the conceptual diagram of the assembly process of COSA. After mounting the components on the package by solder printing and reflow, the chips are mounted. After that, a ball grid array, which is an input/output interface for high-speed electrical and control signals and power supply, is formed. The lid and fibers are then fixed. In this process, full automation of mounting is achieved, contributing to COSA's high productivity and economic efficiency. When mounting on a printed circuit board of an optical transceiver, COSA can be mounted through an automatic surface mount technology (SMT) process together with other electronic components.



Frequency response of transmitter

Frequency response of receiver

Fig. 4. Frequency response of COSA.

Most conventional optical devices require individual mounting processes after an SMT process of electronic components. Therefore, COSA can make the assembly process of a transceiver significantly easier and faster.

4. Next challenge

The APN is a key component of IOWN for introducing photonics everywhere in a communication network. To apply photonics to shorter-distance transmission and even to chip interconnection between an electronic processer, it is necessary to make optical transceiver modules smaller and faster. Currently, only a few analog electronic chips can be integrated in the package of COSA, but larger scale co-packaging will be necessary in the future. It is also required to increase the data rate of the signal transmission.

To further develop and expand photonics-electronics convergence technology, NTT Device Innovation Center is conducting R&D for significantly improving transmission speed of COSA. Compared to 400-Gbit/s transmission, which supports 64-Gbaud signal, we successfully expanded the capable signal baudrate to 100 Gbaud [3]. By expanding the electrical-to-optical (E/O) and optical-to-electrical (O/E) bandwidth of COSA, we significantly improved transmission speed. **Figure 4** shows the improved E/O and O/E bandwidth of the 100-Gbaud class COSA. By improving not only the silicon photonics chip but also the co-packaging technology, the 3-dB bandwidth of the O/E and E/O responses was improved to about 50 GHz.

We confirmed that COSA is a key technology for future ultrahigh-capacity optical networks and that silicon photonics technology will be key for photonics-electronics convergence technology.

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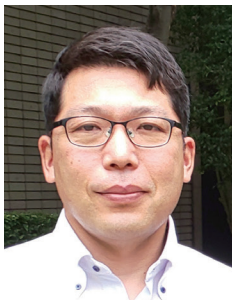

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Device Technology for Short-range Optical Interconnections with High Density and Low Power Consumption

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Abstract

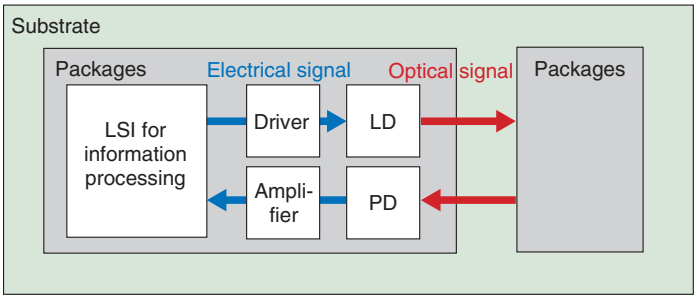
Optical interconnections, which apply optical technology to short-range communications on printed circuit boards in datacenters, are being studied for faster information processing infrastructure and lower power consumption. In this article, we introduce membrane-type directly modulated lasers on silicon (Si) substrates. These lasers can be integrated with Si photonic devices and driven by complementary metal oxide semiconductor-based drivers with low power consumption.

Keywords: photonics-electronics convergence, optical interconnection, semiconductor laser diode

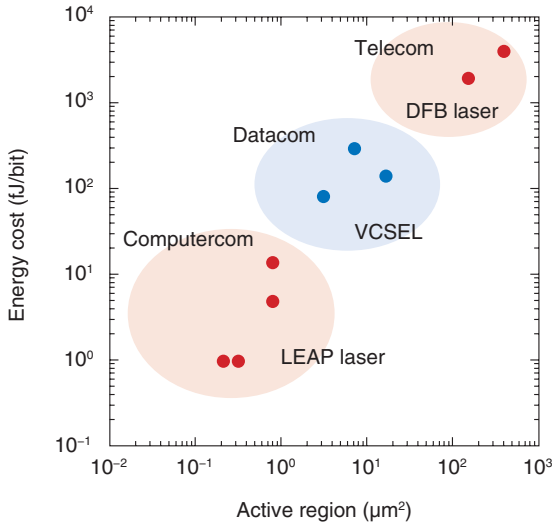
1. Introduction

Due to progress in the Internet of Things and expansion in the use of artificial intelligence, a huge amount of data has been handled, exceeding our expectations, and this trend is expected to continue. It is estimated that the power consumption of information and communications equipment will increase at an accelerated rate as a result of this increase in data processing [1]. If traffic continues to increase and the performance of information and communications equipment does not change, it is predicted that information and communications equipment in 2030 will consume nearly twice today's annual power consumed in Japan. In particular, locations of data processing tend to be concentrated in large datacenters, and the power requirements for datacenters are becoming more stringent at an accelerating data rate. For example, the total power consumption of datacenters in Japan was estimated to be 1% of the annual power consumption in Japan in 2015; thus, it is important to reduce the power consumption for data processing and transmission.

NTT proposed the concept of the Innovative Optical Wireless Network (IOWN) with ultralow power consumption. To achieve this, we are conducting research and development (R&D) on photonics-electronics convergence technology to apply devices used for long-distance communications to short-distance communications. Optical communication technology has been applied to international long-distance communications and domestic metro access networks and has recently been applied to communications between datacenters and between racks and printed circuit boards in datacenters. Electrical wiring, however, is used for communications on such boards and between large-scale integrated circuits (LSIs). The transmission loss increases with the increase in data rate and transmission distance. Optical wiring, on the other hand, is characterized by an almost constant transmission loss and small increase in power consumption while increasing the data rate. NTT is conducting R&D on optical interconnections that apply optical technology to short-range communications on



(a) Block diagram of optical interconnection between LSI chips



(b) Relationship between active region and energy consumption

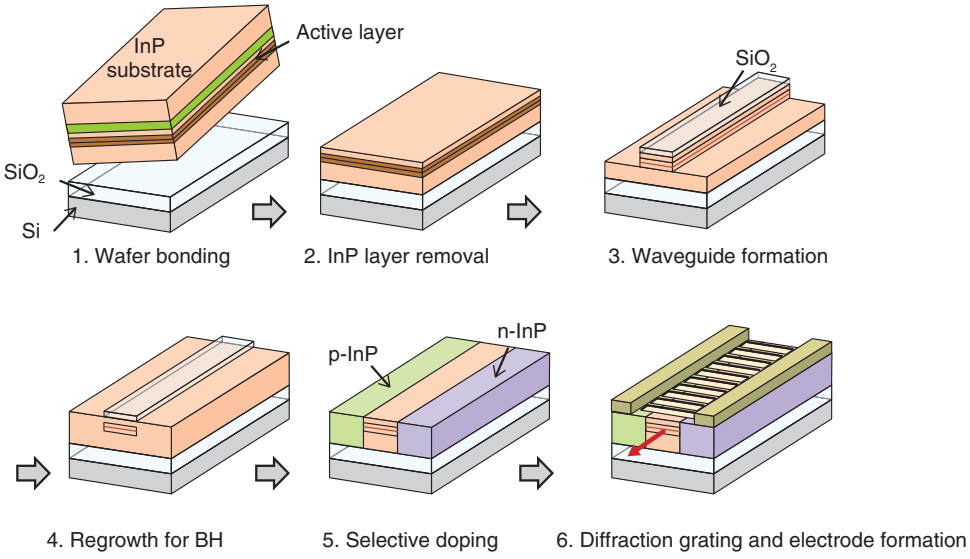
DFB: distributed feedback
LEAP: lambda-scale embedded active-region photonic-crystal
PD: photodiodes
VCSEL: vertical cavity surface emitting lasers

Fig. 1. Block diagram of an optical interconnection between LSI chips and relationship between an active region of a directly modulated LD and energy consumption.

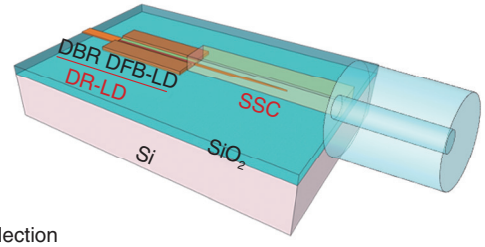
printed circuit boards in datacenters to increase the speed and reduce power consumption of electronic devices used for data processing and transmission.

2. Device technology for short-range optical interconnections

Figure 1(a) shows a block diagram of optical interconnection required for information processing. Optical transmitters and receivers are placed in the vicinity of LSIs to convert electrical signals into optical signals. High-density integration and low power consumption of optical devices, such as semiconductor laser diodes (LDs), are essential to apply optical communication technology to shorter distances. **Figure 1(b)** shows the relationship between the size of the active region and energy consumption of directly modulated LDs used at various distances. In general, when we use LDs with larger active region, larger optical output power can be obtained, although energy consumption is also increased. In telecommunication, large optical power is required for long-distance transmission, and LDs with large active regions are required. The need to reduce energy costs is increasing for data communications such as inter-board transmission. Vertical cavity surface emitting lasers (VCSELs), which are the most widely used light sources in current short-distance communications,



(a) Fabrication procedure for an LD on Si



DR: distributed reflection
SSC: spot size converter

(b) Structure of an LD on Si

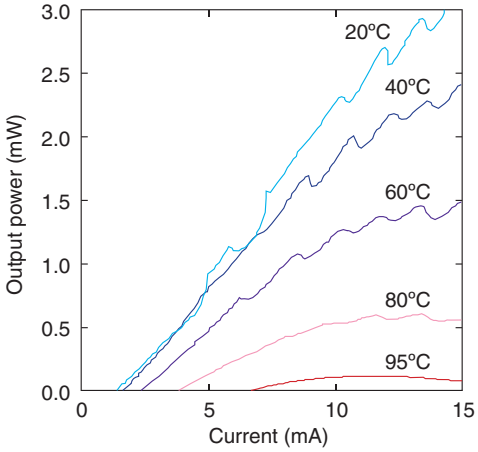
Fig. 2. Fabrication procedure and structure of an LD on Si.

tend to oscillate in multiple modes because of their shape and are not suitable for wavelength division multiplexing (WDM) technology. To increase the transmission capacity, it is necessary to integrate single mode LDs and a wavelength multiplexing circuit. Although VCSELs can shorten the cavity length, which determines the active region, there is a limit to the miniaturization of the active region. NTT is developing thin film (membrane) directly modulated LDs fabricated on silicon (Si) substrates as light sources for on-board optical interconnections. By fabricating LDs on Si substrates, Si photonics technology can be applied to integrate WDM circuits and photodiodes at high density and low cost. In addition, by fabricating LDs on silicon dioxide (SiO_2) layers that have a low refractive index, the LDs can be miniaturized. We can reduce power consumption with this structure owing to the large interaction between light and injected carriers. We are also developing wavelength-scale cavity LDs using photonic crystals to fabricate LDs composed of even smaller active layer regions since the energy consumption of a directly modulated LD is proportional to the size of the active region.

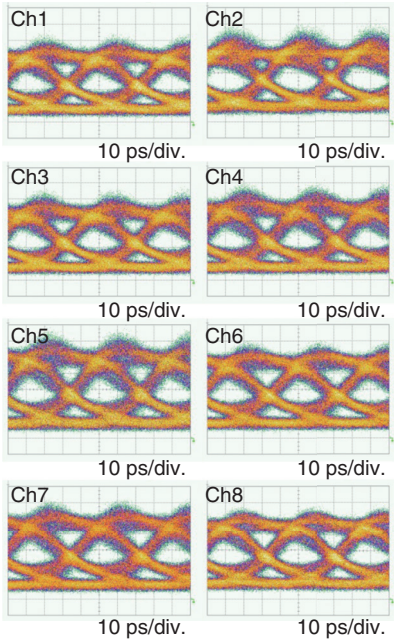
In the following sections, we describe the fabrication and characteristics of LDs on Si substrates and driver circuit design using complementary metal oxide semiconductor (CMOS) technology. We also explain an LD using photonic crystals as our approach for further reducing the power consumption of LDs.

3. Thin film on Si substrate (membrane) directly modulated laser

Figure 2(a) shows the fabrication procedure of an LD on Si substrate [2]. First, optical circuits are formed on Si substrates using Si photonics technologies,



(a) Temperature dependence on bias current vs. optical output power of an LD on Si



(b) Eye diagrams of 8 LDs on Si

Fig. 3. Characteristics of LDs on Si.

then the indium phosphide (InP)-based active layers are bonded to the SiO_2/Si wafer. The active layers consist of indium gallium aluminum arsenide (InGaAlAs)-based multiple quantum wells (MQWs). Mesa stripes are formed by masking the LD regions and etching MQWs. An undoped InP layer is selectively regrown using a metalorganic vapor phase epitaxy to fabricate InGaAlAs/InP buried heterostructures (BHs), which are island-like active layers embedded in thin InP. To inject current into the BHs, n-type and p-type doping regions are formed on either side of the BHs using Si ion implantation and zinc (Zn) thermal diffusion. This structure has advantages in both optical and carrier confinement into BHs. Large optical confinement is achieved owing to the large refractive index contract between the InP and the SiO_2 cladding. Carrier confinement is achieved due to the electrical bandgap difference between the MQWs and surrounding InP that has a bandgap larger than the MQWs. These characteristics make it possible to reduce the size and power consumption of LDs on Si compared to conventional LDs fabricated on InP substrates. The structure of a fabricated LD on Si is shown in **Fig. 2(b)**. The laser-cavity structure is a distributed reflection type that has a distributed Bragg reflector (DBR) on the rear side of the distributed feedback region. The rear DBR allows the lasing light to be selectively emitted from the front of the LD, making the BH smaller. On the front side of the LD, we integrated spot size converters using a SiO_x waveguide, enabling efficient optical coupling with optical fibers.

Figure 3(a) shows the injected current versus optical output power of the fabricated LD. We obtained continuous-wave operation at room temperature with a threshold current of 1.6 mA and lasing wavelength of 1.3 μm. Continuous-wave operation was possible up to 95°C. **Figure 3(b)** shows eye diagrams of eight LDs integrated on the same wafer. The bit rate was 25.8 Gbit/s with the non-return-to-zero (NRZ) format. The energy consumption of a single LD was 200 fJ/bit, which was on the same order of that of VCSELs. WDM circuits can also be integrated monolithically with the same structure [3].

We were successful in fabricating membrane LDs as low-power-consumption light sources that can provide single-mode lasing and have excellent capability for monolithic integration.

4. CMOS driver circuit technology

This section describes the electrical circuits used to

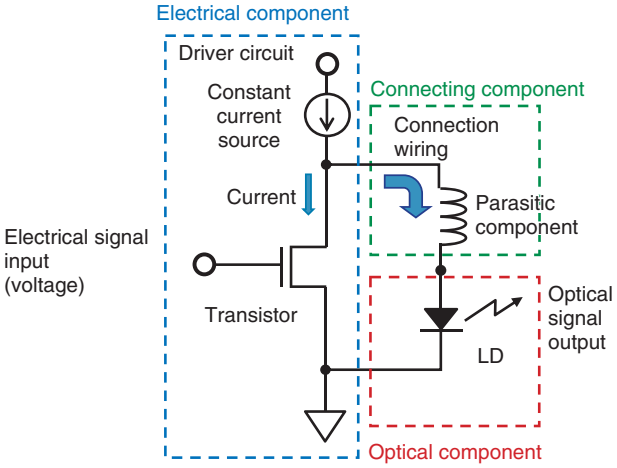


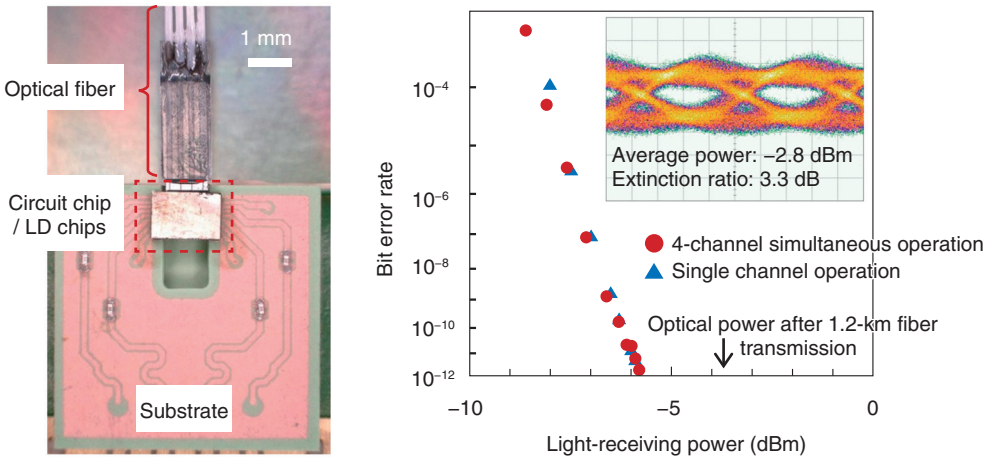
Fig. 4. Configuration and operation of the optical transmitter.

drive the LDs. An LD needs to be driven by an electric current to emit light. However, general digital electric circuits, such as LSIs, operate with voltage as a signal, so a driver circuit is required to convert voltage signal into current. The optical transmitter shown in **Fig. 4** consists of an electrical component (the driver circuit), optical component (LD), and connecting components such as the wiring. This circuit operates as follows. The current from the constant current source is branched (shunt) to flow to either the transistor side or LD side. At this point, when a high-speed electrical signal is input from the left side using a voltage, the transistor acts as a switch and turns on/off. Since the constant-current source continues to supply a constant current, a current flows to the transistor side when the transistor is turned on. Less current flows to the LD side, and no light is emitted. When the transistor is turned off, however, current flows to the LD side, and light is emitted. Therefore, the light emission of an LD can be turned off and on by turning on and off the transistor.

The requirements for driver circuits are high-speed operation, low power consumption, and small size. To meet these requirements, we selected CMOS technology to fabricate the transistors and applied our core opto-electronic integrated design technology [4] to the electrical circuits. It was necessary to fabricate a prototype of the optical transmitter, measure the characteristics of the electrical and optical components, and redesign to tune the parameters of the components. With our opto-electronic integrated design technology, we constructed a model in which the optical and connecting components are replaced with an electric equivalent circuit. By incorporating this model into the field of electrical circuitry where simulation and design tools are mature, it is possible to make performance predictions through integrated design.

Next, we describe a small mounting structure of the optical transmitter (**Fig. 5(a)**). For the electrical connection, the surface of the CMOS driver circuit chip is mounted on the surface of the LD chip. This not only reduces the chip area but also shortens the electrical-wiring connection, reducing the parasitic inductance and allowing high-speed signals to pass through. For optical connections, we connected a 4-channel optical fiber array directly to the end facet of the LD chip with a width of 1 mm, enabling small and low-loss optical connections.

The characteristics of the optical transmitter are shown in **Fig. 5(b)** [5]. A pseudo random bit string (7 steps) with a bit rate of 25 Gbit/s NRZ is input to each channel, and the transmitter consists of 4 channels to achieve a transmission capacity of 100 Gbit/s. The inset shows the eye diagram of the optical signal output from one channel, and we obtained an eye opening with an extinction ratio of 3 dB or more. As a result of evaluating the bit error rate after propagating a standard single mode fiber of 1.2 km, we confirmed that error-free transmission (bit error rate $< 10^{-12}$) can be achieved even when four channels are simultaneously driven. Since the total power consumption of the optical transmitter is 267 mW, the power efficiency is 2.67 pJ/bit, and low power consumption was achieved.



(a) Mounting structure (b) Evaluation results (channel #1)

Fig. 5. Fabricated optical transmitter.

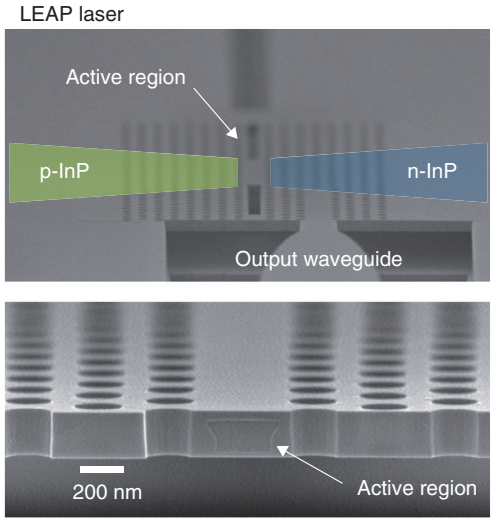
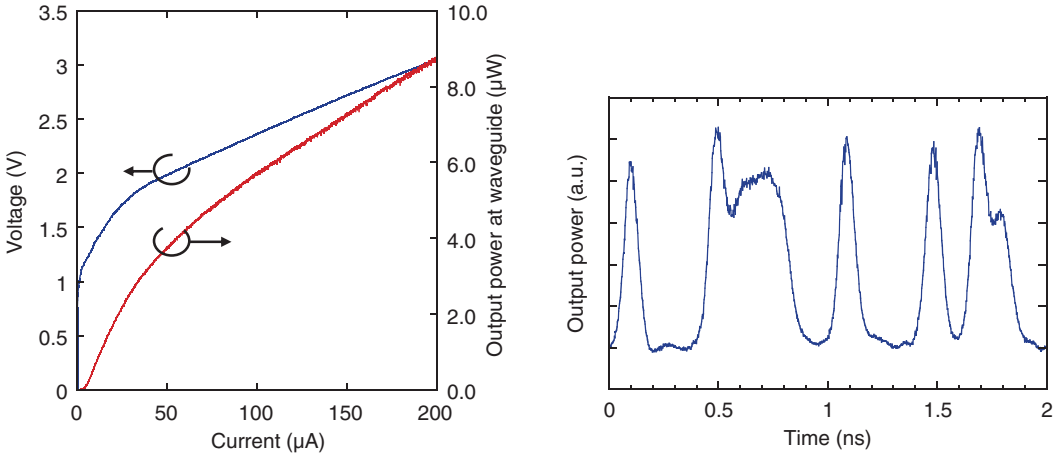


Fig. 6. Scanning electron microscopy images of a LEAP laser.

5. LEAP lasers

As explained in Fig. 1(b), further reduction in energy consumption is required for interconnection on printed circuit boards and between chips, and LDs with small active area are required. NTT developed small LDs using photonic crystals [6]. **Figure 6** shows scanning electron microscopic images of one of these LDs. Photonic crystals are artificial periodic structures, and the periodicity of refractive index is the same as the wavelength of light. This structure allows the light to be localized very strongly in the designed region. We fabricated these LDs with an active layer embedded in an InP photonic crystal by using BH technology. We call these LDs lambda-scale embedded active region photonic crystal (LEAP) lasers because of their structure.

Figure 7(a) shows the injection current versus optical output power of a LEAP laser at room temperature. Even with such a small LD, we achieved continuous-wave operation at room temperature and a record low threshold current of 4.8 μA. **Figure 7(b)**



(a) Injection current-optical output characteristics of a LEAP laser.

(b) Optical waveform of a LEAP laser for 10-Gbit/s NRZ direct modulation

Fig. 7. Characteristics of a LEAP laser.

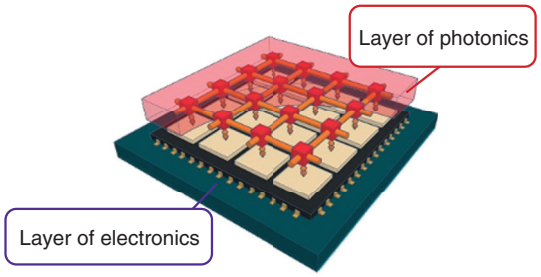


Fig. 8. Photonics-electronics convergence chip for information processing (optical interconnection between cores in the chip).

shows a direct modulation waveform with an NRZ signal of 10 Gbit/s at a bias current of 25 μA. Direct modulation was possible even with such a small bias current, and a record low-energy consumption of 4.4 fJ/bit was achieved with a single LD.

Therefore, we demonstrated that power consumption can be much lower with LEAP lasers. LEAP lasers can be formed not only on InP substrates but also on Si substrates by combining them with the bonding technology described in the previous section.

6. Future developments

The semiconductor LDs on Si substrates introduced in this article can be integrated with Si photonic devices and driven with low power consumption by using a CMOS driver. We will continue to strive for higher transmission capacity and higher density integration and further advance integration with information processing circuits such as in central and graphics processing units (**Fig. 8**). We will also conduct further research and development to contribute to the development of future information processing infrastructure.

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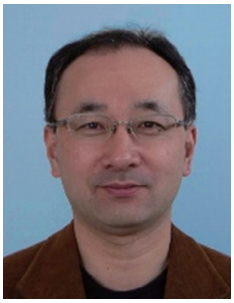

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Nanophotonic Technologies toward Opto-electronic Integrated Accelerators

Kengo Nozaki, Akihiko Shinya, and Masaya Notomi

Abstract

The opto-electronic integration technology being researched at the NTT Nanophotonics Center is for creating a photonic computing platform with low latency and low energy consumption. The development of miniature optical functional devices through nanophotonics along with advances in large-scale optical-circuit fabrication technology will make diverse types of photonic-information processing possible. This article introduces the technologies that we are researching for optical pass-gate circuits, opto-electronic converters, and optical nonlinear devices and presents the path to *opto-electronic integrated accelerators* that the combined use of these technologies will make possible.

Keywords: opto-electronic integration, photonic computing, photonic crystal

1. Optical technology: from communication to processing

Optical technology is currently the driving force behind large-capacity information transmission including long-haul optical fiber communication and inter-server communication in datacenters. By extension, progress in optical communication for shorter distances can be considered but will ultimately mean optical networking on a computer chip and information processing based directly on light. Developing an optical computer has been one of the major goals of researchers in the field of optics, but the mature complementary metal-oxide semiconductor (CMOS) electronic circuit technology has prevented any meaning from being found in using light in computing. However, CMOS-based nano-fabrication and circuit integration are gradually approaching their limits, so expectations are increasing for information processing using the high-speed properties of light [1]. These expectations are being boosted by progress in miniature and energy-saving optical device and circuit technology made possible by fine-processing technology called *nanophotonics*. Recent advances in silicon photonics technology are also generating strong synergy with nanophotonics, and the implementation of a large-scale optical circuit in a compact space is expanding the opportunities for photonic computing research.

Though it is generally difficult to carry out various types of information processing solely with optical circuits, importance is being given to an accelerator that can accelerate specific processing by combining optical circuits with the parallel digital processor and large-capacity memory of CMOS electronics and enabling optical circuits to carry out high-speed-specific processing applicable to light [2]. In particular, the value of using light has been reevaluated recently as extending beyond digital processing to include analog processing as in machine learning and photonic microwave-signal processing, and an opto-electronic integrated accelerator that links CMOS electronics and nanophotonics has begun to take form.

The following introduces a low-latency optical pass-gate circuit, opto-electronic converters, and an optical nonlinear device as three key components deemed essential to developing an opto-electronic integrated accelerator (**Fig. 1**).

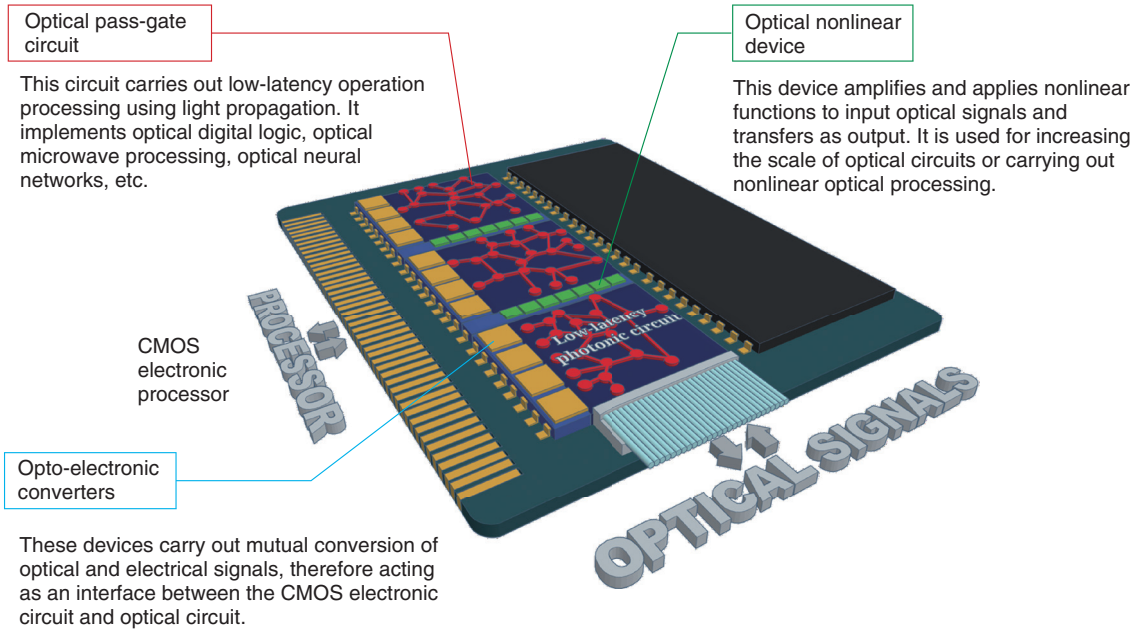

Fig. 1. Conceptual schematic of an opto-electronic integrated accelerator.

2. Low-latency optical pass-gate circuit

The barrier to the continuation of Moore's law in CMOS electronic circuits (empirical rule stating that performance improves due to finer processing and greater integration) is the increase in signal delay and heat generation as a result of resistance and capacitance of transistors and metal wiring. In electronic circuits, digital logic operations, such as AND-OR-INVERT logic, are carried out by cascaded connection of logic gates. A subsequent gate waits for the signal output from a prior gate so that the time delay to obtain the calculation result increases proportionally to the number of gate stages. In addition, increasing the signal bit rate increases heat generation due to an increase in the movement of free electrons in metal. As a consequence, the signal bit rate of CMOS electronics for computing that requires low power consumption has generally been held to several gigahertz. For these reasons, the current situation is that, while processing capacity (throughput) can be increased through further increases in CMOS fine processing and integration, processing delay (latency) is hitting a ceiling.

As shown in **Fig. 2**, an optical pass-gate circuit consists of the integration of optical switches that switch optical transmission paths. In the example shown in Fig. 2(a), calculation results are output by triggering Mach-Zehnder interferometer optical switches* at the same time by signals from the electronic circuit and transmitting light along the selected paths as light beams interfere with each other. There is no power loss or heat generation due to resistance, as in the case of electronic circuits, and calculations are carried out through the interference of light, which opens the door to low-energy and low-latency processing. We can take as an example a full-adder circuit that inputs digital signals ("1" and "0" binary signals). The calculation of the carry signal from least-significant bit to most-significant bit constitutes the adder's *critical path* that determines total delay. However, carrying out such processing using optical pass-gates is expected to reduce delay compared with that of electronic circuits [3]. Therefore, optical pass-gates should be applicable to other digital operations including basic arithmetic operations.

In addition to digital processing, progress is also being made in analog processing (carried out with continuous values). In particular, there are high

* Mach-Zehnder interferometer optical switch: A switch that splits light into two beams and applies voltage to one, thereby changing the refractive index of that waveguide and changing the phase of light. It then determines the light output by having the two light beams interfere with each other (see Fig. 2). Digital processing determines the output ratio to be either 0/1 or 1/0, while analog processing results in a continuous output ratio from 0 to 1.

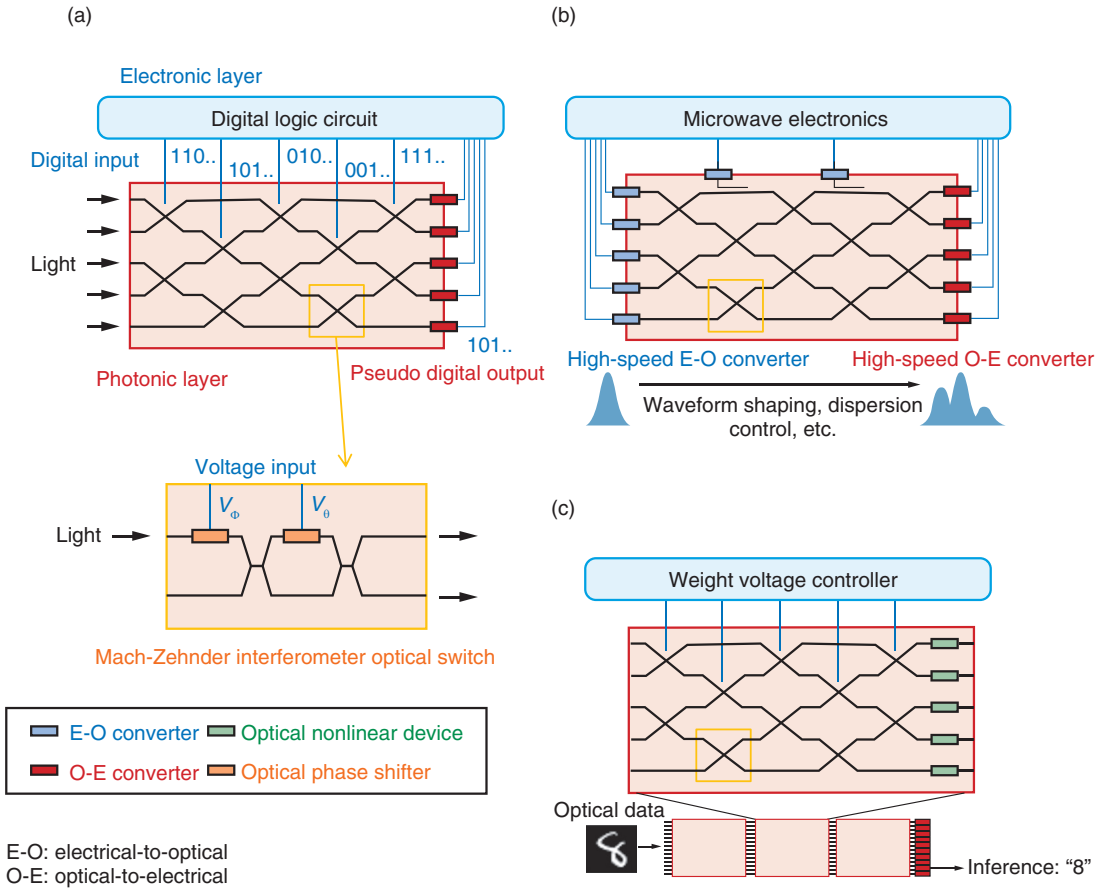

Fig. 2. Example of optical pass-gate circuits: (a) optical digital logic processing, (b) optical microwave processing, (c) optical neural network.

expectations for microwave photonics technology to convert microwave signals used in wireless communications to light, execute processing that requires high spectral resolution and temporal resolution (filtering, waveform control, dispersion control, etc.) in the optical domain, and output the results again as microwave signals (Fig. 2(b)) [4]. At the same time, research on optical neural networks is becoming quite active worldwide along with advances in deep learning and other artificial intelligence technologies. At the core of this analog processing is vector-matrix multiplication (VMM), but its calculation cost has been a bottleneck in CMOS digital circuits. On the other hand, a pass-gate circuit based on light interface can be used to physically implement VMM, so a solution to these problems is expected [5]. The possibility exists of achieving low-latency inference by combining this optical pass-gate circuit with an opto-electronic converter and optical nonlinear device, as described below, to configure opto-electronic neural network integration (Fig. 2(c)).

3. Opto-electronic converters (interface between optical and electronic circuits)

A major issue in integrating CMOS and optical circuits is developing a high-density opto-electronic interface featuring a miniature and energy-saving electrical-to-optical (E-O) converter, i.e. an electro-optic modulator (EOM), and optical-to-electrical (O-E) converter, i.e. a photodetector (PD). We have been developing such converters using nanostructures called photonic crystals (**Fig. 3**), which are periodic structures formed in semiconductors. They can be used as ultrasmall optical waveguides and optical resonators by forming periodic airholes with diameters of ~200 nm on a thin semiconductor plate and arranging their layout. At NTT, we developed

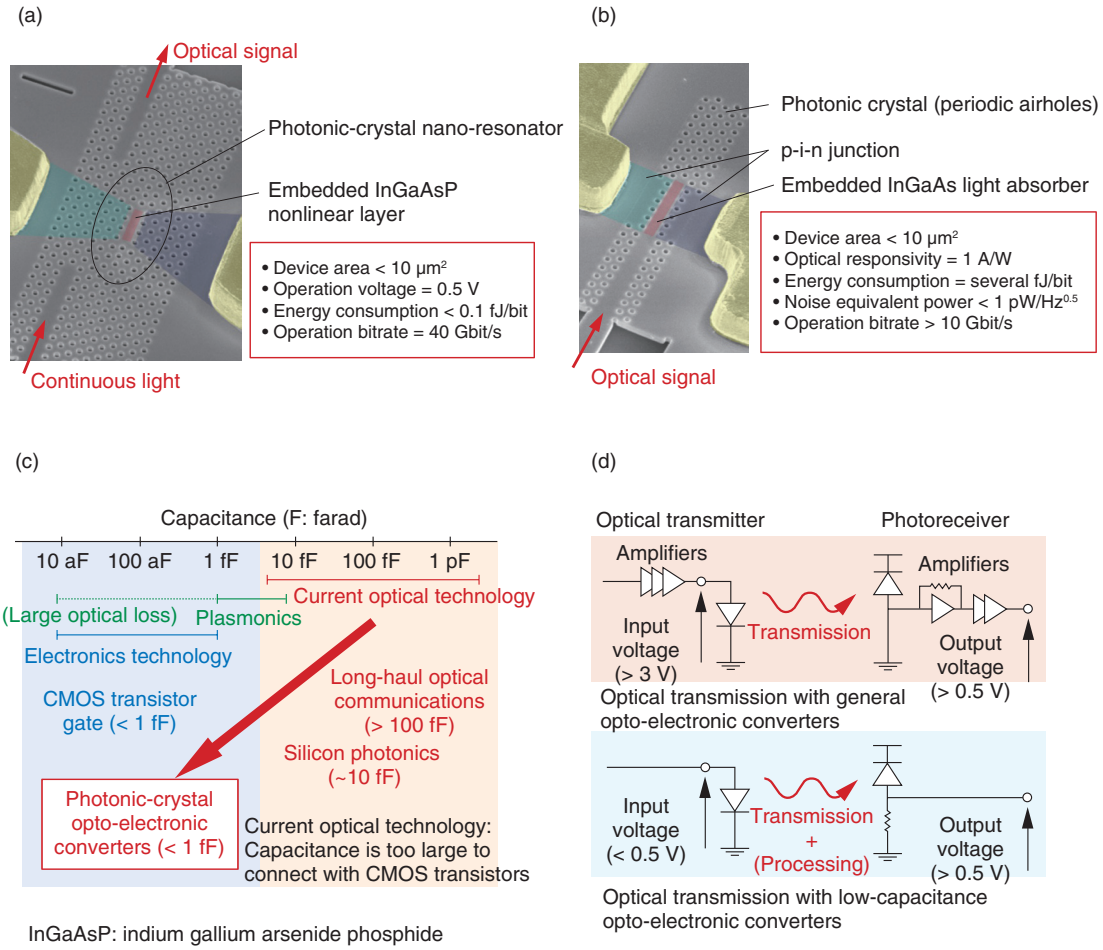

Fig. 3. Performances of opto-electronic converters using photonic crystals: (a) nanophotonic EOM, (b) nanophotonic PD, (c) comparison of device capacitance, and (d) simplification of optical communication circuit with low-capacitance opto-electronic converters.

functional devices such as optical switches, optical memory, and laser sources and demonstrated record-low energy operation. We also demonstrated E-O and O-E converters, i.e., a nanophotonic EOM and PD, as shown in Figs. 3(a) and (b), and succeeded in dramatically reducing the size and energy consumption of these converters compared with those of conventional ones [6].

For E-O/O-E converters, the low electrical capacitance can be an important figure of merit. As shown in Fig. 3(c), the capacitance of a single CMOS transistor is less than one femtofarad (fF), whereas that of conventional E-O/O-E converters is generally large, i.e., 10 fF or greater. This requires high energy consumption in proportion to the large capacitance, creating a bottleneck. On the other hand, our converters can reduce capacitance to less than 1 fF, the same as that of CMOS transistors. Such a capacitance reduction is of major significance. As shown in Fig. 3(d), optical communication based on conventional E-O/O-E converters requires multiple amplifier stages to generate a sufficient voltage signal, which increases power consumption and device area. In contrast, the electrical energy required for logic operations in CMOS transistors can be sufficient to drive our low-capacitance converters, enabling seamless opto-electronic integration requiring no amplifiers. We therefore expect our converters to be used for configuring dense optical networks either between or within CMOS chips based on simple optical transceiver circuits with a strong energy-saving effect and for even optical-signal processing within communication. Going forward, the key to these advances is integrating CMOS and opto-electronic converters

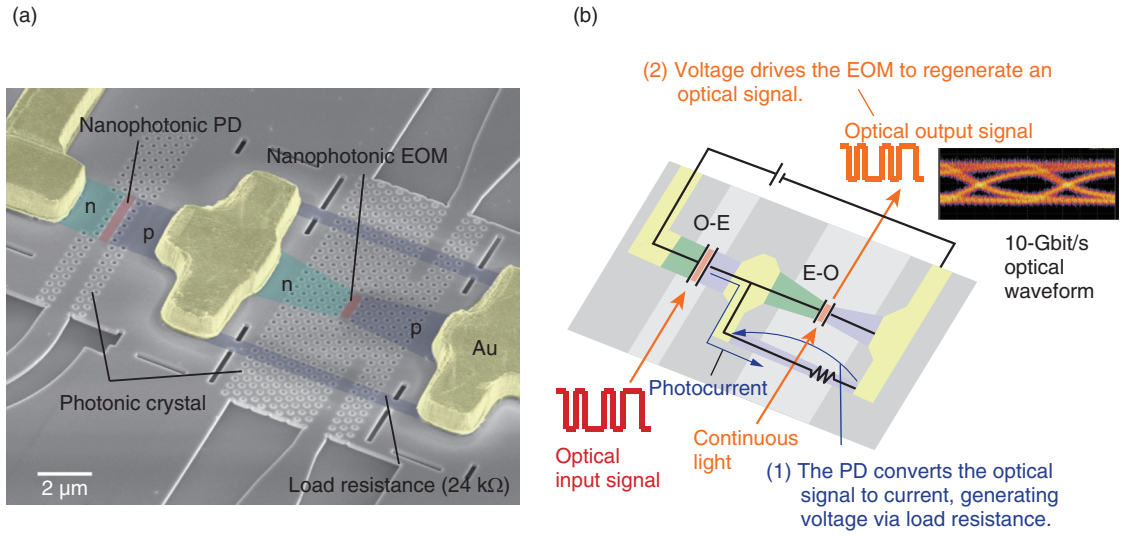

Fig. 4. Optical nonlinear device (optical transistor): (a) photo of device, (b) operation principle.

while maintaining low capacitance and developing opto-electronic interfaces toward practical computing applications.

4. Optical nonlinear device (optical transistor)

Nonlinear operations such as signal switching and amplification, as in electrical transistors, play an important role in optical circuits. However, though light is particularly good at linear signal processing based on light interference, nonlinear signal processing generally requires strong light-matter interaction, which in turn requires high optical energy. To overcome this, we fabricated an O-E-O converter by integrating the nanophotonic PD and EOM described above, and developed an energy-saving optical nonlinear device (**Fig. 4**). The optical input signal to the PD is converted to current that is then converted to a voltage via load resistance (24 kΩ). This voltage, in turn, drives the EOM so that the input signal waveform is transferred to another light. This results in nonlinear signal transfer at 10 Gbit/s. With this operation, the optical output power from the EOM is at least two times greater than that of the optical input power at the PD. It can be said that we have achieved an *optical transistor* producing an optical signal gain in the same manner that an electrical transistor produces an electrical signal gain [7].

The electrical capacitance of this opto-electronic integrated device is extremely small at 2 fF, and such integration that maintains ultralow capacitance is the world's first. Current O-E-O converters suffer from large capacitance, making energy consumption substantially high, but our low-capacitance device reduces this to several fJ/bit, which is less than 1/100 that of current devices. The fact that this device exhibits optical signal gain should enable multi-stage transfer of optical signals. Thus, it should be possible to connect and increase the scale of optical pass-gate circuits. We can also envision its applications including its use as a nonlinear optical neuron in the optical neural network shown in Fig. 2.

5. Conclusion

There are options to maximize the superior features of light and obtain a level of performance that exceeds that of electronic circuits. The ability of multiplexing optical information by wavelength, space, and time to increase the dimensions of processing provides a significant advantage over electronic processing. Practically, we need an opto-electronic co-design that takes into account opto-electronic converters, analog-to-digital converters, and the latency and energy efficiency within electronic circuits. An approximate computing design that balances accuracy and computing cost is becoming increasingly important [8]. Beyond the device technology (component level) introduced in this article, a broader perspective (architecture level) is required to discover the specific form that opto-electronic integrated computing should take.

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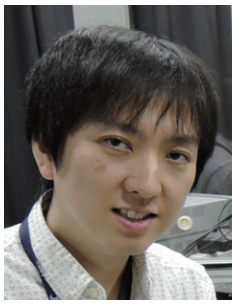

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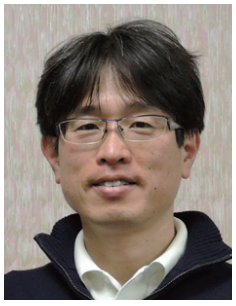

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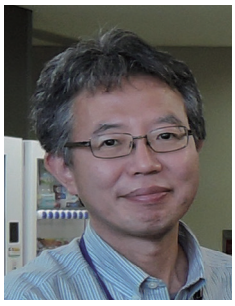

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Ultralow Latency Optical Logic Operations with an Ultrasmall Silicon Wire Ψ Gate

Shota Kita, Kengo Nozaki, Kenta Takata, Akihiko Shinya, and Masaya Notomi

Abstract

Electronic computation circuits are composed of logic gates. However, due to the exponential increase in wiring resistance of miniaturized electronic components, both the increase in latency and energy consumption is becoming a serious problem. To overcome the electronic bottleneck, we developed an ultrasmall silicon-wire multimode interferometer called a *Ψ (psi) gate* for low-loss and high-speed optical logic operation. With a single Ψ gate, we can carry out Boolean logic operations (OR, XOR, AND, XNOR, NOR, and NAND) in telecom wavelength (1535–1565 nm) with an ultralow latency of ~30 fs. Such gates are expected to be used in novel photonics-electronics convergence processors for ultralow latency pattern matching and vector operations for photonic neural network applications.

Keywords: optical logic gates, linear optics, silicon photonics

1. Introduction

Data processing infrastructures based on complementary metal oxide semiconductors (CMOS) have seen continuous growth owing to the huge progress in semiconductor fabrication technologies. However, increases in leakage current and wiring resistance due to the miniaturization of electronic circuits will put an end to this continuous growth in the near future [1]. Accordingly, we are seeing accelerated exploration of novel technologies in all domains of science and technology towards the next generation of scalable data processing infrastructure. Moreover, latency has been worsening because the increase in wiring resistance also limits the response speed of electronic circuits (known as resister-capacitor time constant), which would limit the future development of applications related to communications security, real-time control, financial transactions, and so on. Note that latency can be reduced by inserting repeaters in electronic wires. This method is not energy efficient and would not help to overcome the traditional trade-off between latency and energy consumption.

It is expected that this latency problem can be drastically mitigated using light for processing not only for communication because an optical signal can propagate through photonic circuits at the speed of light. Additionally, if the elemental photonic devices comprising a photonic circuit become smaller, the total optical pass length in the circuit will become shorter. Thus, further reducing device size lowers latency [2]. Our group developed high-performance micro/nanophotonic devices, e.g., nanolasers [3], nanophotodetectors [4], nanomodulators, and optical transistors [5], which should be fundamental building blocks for fabricating low-latency nanophotonic processors. We also developed the first high-performance ultralow-latency optical logic gate based on light-interference, called a *Ψ (psi) gate* based on its shape (**Fig. 1(a)**), as another building block [6].

In this article, we introduce the concept and a brief theoretical background of Ψ gates and the experimental demonstration of various optical logic operations with a single Ψ gate. We also present preliminary

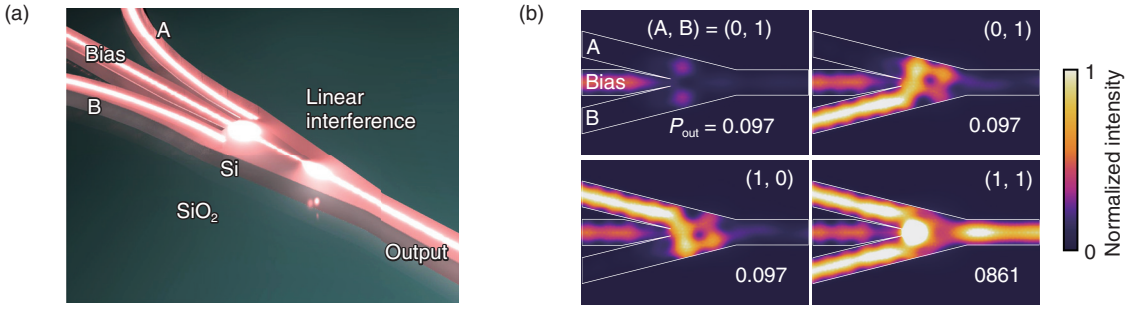

Fig. 1. A Si wire Ψ gate. (a) An illustration of Ψ gate operation. (b) An example of simulated AND logic operation (λ = 1.54 μm). The horizontal white bar at bottom-right inset indicates a 1-μm-long scale bar.

on-chip integration of a Ψ gate and other photonic components for stable operation. Next, we show how to use Ψ gates for optical multibit AND circuits and estimate latency, which is 10 times lower than the best case of CMOS electronic circuits. Finally, we conclude with the potential of using Ψ gates in ultralow-latency photo-electronic-converged accelerators.

2. Logic operations with a silicon wire Ψ gate

Light-interference is a linear phenomenon, so it has been too primitive to carry out various logic operations, and the functions and performance were limited. However, almost all representative Boolean logic operations can be carried out with a single linear gate by introducing the concept of bias light and adjusting the input conditions [7]. Such multiple interference systems can be implemented using silica planer lightwave circuits [8], silicon (Si) photonics [9], and plasmonics [10]. The footprint of the gates is crucial for dense integration. Therefore, if we only need to make it as small as possible, we should choose plasmonics as the platform. However, we need to consider insertion loss to consider the configuration for multibit operations (discussed in Section 5). We found that the most promising platform is Si photonics.

Our Ψ gate (Fig. 1(a)) has three input ports and one output port (the Ψ gate is a part of a 3 × 3 interferometer with two extra hidden radiation ports). Two of them are signal ports (A and B), and the center one is a bias port (denoted as Bias). The two sequences of the intensity modulated signals are input into A and B (relative input powers of both signals P_A and P_B are varied between P_0 and P_1) with a fixed relative phase relationship. In contrast, the intensity of the bias light is fixed at P_{Bias}. The optical output signal power P_{out} through a Ψ gate is then given as follows [6];

$$P_{out} = (\sqrt{P_A T_A} + \sqrt{P_B T_B}\cos\Delta\Phi + \sqrt{P_{Bias} T_{Bias}}\cos\Delta\Phi_{Bias})^2 + (\sqrt{P_B T_B}\sin\Delta\Phi + \sqrt{P_{Bias} T_{Bias}}\sin\Delta\Phi_{Bias})^2, \quad (1)$$

where T_X is the transmittance from each input port X to the output port (satisfying $T_A + T_B + T_{Bias} \leq 1$ due to the linearity), and $\Delta\Phi$ and $\Delta\Phi_{Bias}$ are the relative output phases of B and Bias to the output of A, respectively. Within this degree of freedom, for example, we can implement an optical AND logic operation, as shown in **Fig. 1(b)**.

In this situation, we set $T_A = T_B \sim 0.39$, $T_{Bias} \sim 0.20$ ($T_A + T_B + T_{Bias} \sim 0.98$), $\Delta\Phi = 0$, $\Delta\Phi_{Bias} = \pi$, and $P_{Bias} \sim 0.48$ for the maximum binary contrast (*BC*) of 9.54 dB [7]. From the simulated intensity distributions of Fig. 1(b), the operation result appears just after the multiple interference part of the Ψ gate. This means the AND operation is carried out by just passing the light through the 3-μm-long Ψ gate. Therefore, the physically limited computation latency of a single AND operation is ~30 fs. This latency is more than 100 times lower than that of CMOS electronics (~10 ps). From the P_{out} of (A, B) = (1, 1), we define signal loss (*SL*) as $10\log_{10}(P_{out}/P_1)$ (*SL* becomes 0 dB when $P_{out} = P_1 = 1$). By using the Si photonics platform, we can obtain *SL* < 0.5 dB. Even if we try to fabricate a similar interferometer based on loss-less half mirrors, *SL* becomes ~1.25 dB. As far as we know, there have been no reports on optical logic gates with such low *SL*. The required relative bias power P_{Bias}/P_1 for the maximum *BC* for an AND operation can be derived from Eq. (1) as follows;

Table 1. Optical input/output table for linear optical logic gate operations in silicon wire Ψ gates with and without bias input.

P_A	P_B	$\Delta\Phi$	0	π	$2\pi/3$	0			$2\pi/3$
		P_{Bias}/P_1	0			$T_A/4T_{Bias}$	T_A/T_{Bias}	$9T_A/4T_{Bias}$	T_A/T_{Bias}
		$\Delta\Phi_{Bias}$	–			π			$-2\pi/3$
0	0		0	0	0	$T_A/4$	T_A	$9T_A/4$	T_A
0	1		T_A	T_A	T_A	$T_A/4$	0	T_A	T_A
1	0		T_A	T_A	T_A	$T_A/4$	0	T_A	T_A
1	1		$4T_A$	0	T_A	$9T_A/4$	T_A	T_A	0
				XOR	OR	AND	XNOR	NOR	NAND
BC [dB]			6	∞	∞	9.5	∞	9.5	∞

$$\frac{P_{Bias}}{P_1} = \frac{T_A}{4T_{Bias}}\left(1 + 3\sqrt{\frac{P_0}{P_1}}\right)^2 \quad \text{(for AND).} \quad (2)$$

Here, P_{Bias}/P_1 is determined from the ratio of T_A and T_{Bias}. Larger T_A gives larger P_{out} (smaller *SL*); on the other hand, P_{Bias}/P_1 becomes larger (larger total input power into a Ψ gate). In the case of Fig. 1(b), we balance T_A and T_{Bias} according to the minimization of net loss [6]. By keeping the same $\Delta\Phi$ and $\Delta\Phi_{Bias}$, P_{Bias}/P_1 for XNOR and NOR operations can be derived as follows;

$$\frac{P_{Bias}}{P_1} = \frac{T_A}{T_{Bias}}\left(1 + \sqrt{\frac{P_0}{P_1}}\right)^2 \quad \text{(for XNOR),} \quad (3)$$

$$\frac{P_{Bias}}{P_1} = \frac{T_A}{4T_{Bias}}\left(3 + \sqrt{\frac{P_0}{P_1}}\right)^2 \quad \text{(for NOR).} \quad (4)$$

This means we can switch AND, XNOR, and NOR logic operations by only adjusting P_{Bias}. All the representative logic operations can be implemented, as shown in **Table 1**, by adjusting the input conditions. In terms of cascade connection, it only allows linearly separable combinations (e.g., multibit AND, multibit NOR, etc.). To expand functionality, it is necessary to apply some nonlinearity by inserting optical-electronic-optical conversions through optical transistors [5].

3. High-speed optical logic operations

A sample of a silicon wire Ψ gate was fabricated on a silicon-on-insulator (SOI) substrate with a 220-nm-thick top Si layer. An e-beam resist was spin-coated on the substrate, and the resist pattern was formed after e-beam writing and development. The resist pattern was transferred to the Si layer by using dry etching. After the resist was removed, polymer spot size converters [11] were fabricated for the input/output ports by using 2nd e-beam lithography.

Figure 2 illustrates our setup for demonstrating high-speed logic operations. We used several off-chip optical components connected with several fiber patch cords. However, the relative phases of the input signals are always affected by phase fluctuations due to the mechanical vibrations of the fibers. To eliminate such fluctuation, we used fiber stretchers controlled using a digital proportional integral differential (PID) regulator. First, the laser light was split into two using a tunable coupler. One is intensity-modulated input for signal ports A and B, and the other is an invariant input for the bias port. To generate arbitral optical bit patterns, an optical transmitter connected to a pseudo random pulse pattern generator with a radio-frequency signal multiplexer was used (up to 64 Gbit/s). The generated optical bit patterns were separated into two by using a 3-dB coupler. After intensity tuning with a multi-channel variable optical attenuator, the bottom-side signal was delayed using a fiber delay line so that the Ψ gate under the test effectively had two different pseudo random bit patterns for signal ports A (top-side) and B (bottom-side). All the input and output lights were coupled to the SOI chip by using a lens module and lensed fiber. The output light was amplified through an erbium-doped fiber amplifier. After removing the amplified spontaneous emission noise by using an optical band-pass filter, the output bit patterns were observed using an optical sampling oscilloscope with a bandwidth of 70 GHz. For the optical phase lock loops between signals and bias light, we obtained an individual phase difference between signals and a bias light (the bias channel is set as the phase standard). The phase of the bias light was weakly modulated using the fiber-input phase shifter (PS) with 200 kHz for the dithering. The converted electrical signals through two channels of the photo receiver were input to a

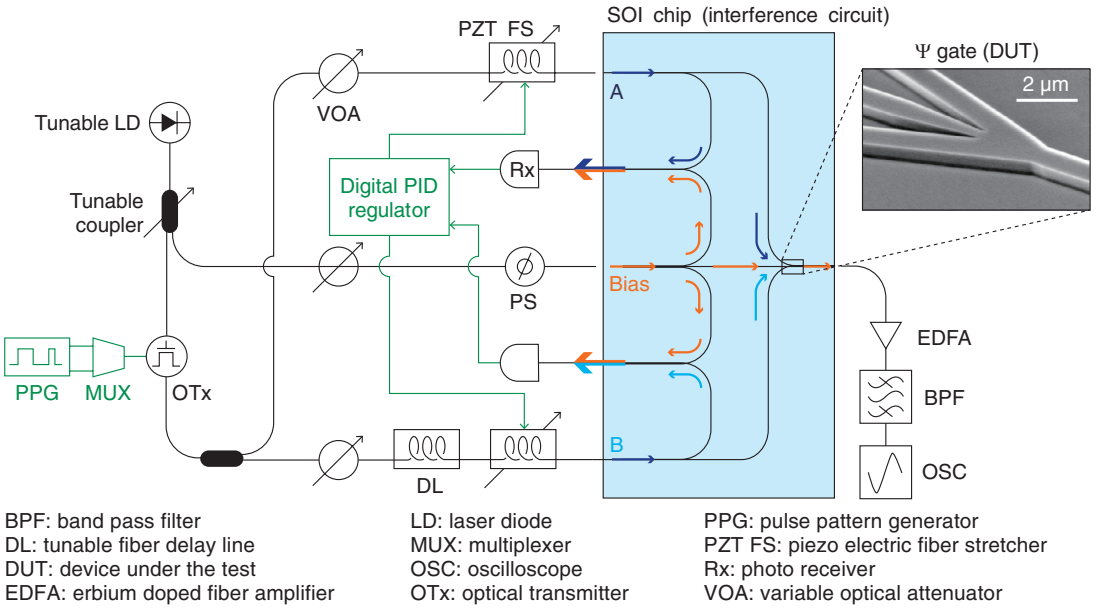

Fig. 2. Experimental setup for verifying high-speed operation of Ψ gates. The inset shows a scanning electron microscope image of the measured Ψ gate.

digital PID regulator. This PID regulator includes a high-voltage amplifier for directly driving the fiber stretcher.

Figure 3 summarizes various logic operations obtained from a single Ψ gate. The output power of the tunable laser diode was set to 8 dBm for the demonstration. Figure 3(a) shows the input and output optical time waveforms of 10-Gbit/s XOR, OR, AND, XNOR, and NOR logic operations with proper input conditioning according to Table 1. We clearly demonstrated the basic concept of the linear optical logic operations. The XOR and OR operations do not require the bias input. In our demonstration, however, a fraction of P_{Bias} was required for optical phase locking. The AND, XNOR, and NOR operations exhibit *BC* of ~9.3 dB, > 10 dB, and ~9.0 dB with P_{Bias}/P_1 ~ 0.62, 1.6, and 3.1, respectively. The experimental P_{Bias}/P_1 fits well to the analytical prediction of Eqs. (2)–(4) by taking into account the finite extinction ratio (*ER*) of the input signals ($ER = 10 \log_{10}(P_1/P_0)$ ~ 13–23 dB). Figure 3(b) shows the case for 40-Gbit/s pseudo random bit sequence AND and NOR operations. Both operations seemed to work with some degradation because of the finite rise/fall time of the input signals (~30 ps). However, the Ψ gate never became the bottleneck of the operation bandwidth because of the quite flat spectral response over 100 nm in the wavelength [6]. Figure 3(c) illustrates a 10-Gbit/s *wavelength insensitive* AND operation in telecom wavelength (1535–1565 nm). By calibrating P_{Bias}/P_1 for each λ, a similar *BC* was achieved for all the tested input wavelengths. In this demonstration, the input signal bit sequences and operations were the same for all λ. It should be noted, however, that we can simultaneously carry out different operations for each wavelength channel by varying the input conditions (that is, totally independent parallel logic operations are possible up to the number of input channels with a single Ψ gate). This is unique and benefits our linear gates compared to nonlinear gates. Note that the demonstrated input wavelength range was actually limited by our setup, and the flatness of the transmission spectra and optical damage threshold should be improved by applying further structural optimization of Si wire Ψ gates. Ultimately, massive-parallel operations are expected to be carried out with more than several dozen wavelength channels in the 1400–1600 nm wavelength range.

4. Preliminary on-chip integration with PSs

Towards practical applications, it is important to show the feasibility of the on-chip integration to demonstrate the phase stability without any optical phase lock loops. Therefore, we also fabricated a Si Ψ gate with several thermo-optic PSs, as shown in **Fig. 4(a)**.

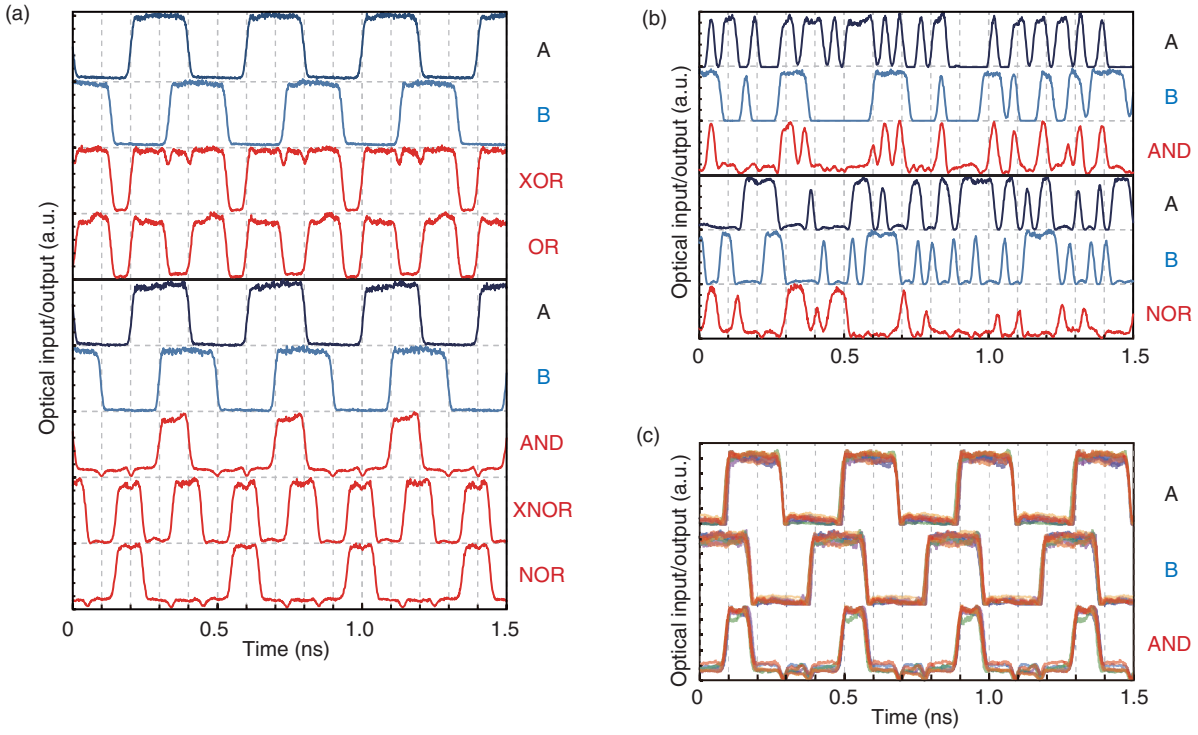

Fig. 3. Experimental linear optical logic operations observed with a single Ψ gate. (a) Time waveforms of optical input signals and outputs demonstrating 10-Gbit/s XOR, OR, AND, XNOR, and NOR logic operations. (b) Time waveforms of optical input signals and outputs demonstrating 40-Gbit/s pseudo random bit sequence AND and NOR logic operations. (c) Time waveforms of optical input signals and outputs demonstrating input wavelength-insensitive 10-Gbit/s AND logic operations. Colors denote different input wavelengths (purple: 1535 nm, blue: 1540 nm, light blue: 1545 nm, green: 1550 nm, orange: 1555 nm, red-orange: 1560 nm, red: 1565 nm).

For each arm, a pair of a Mach-Zehnder modulator (MZM) and PS are inserted to generate signals A and B, and P_{Bias}, $\Delta\Phi$ and $\Delta\Phi_{Bias}$ are adjusted. After conditioning all nine heaters, each MZM was operated with two different frequencies (2 and 1 kbit/s). Then nearly ideal AND and NOR operations with a *BC* of ~9.5 dB were demonstrated, as shown in **Fig. 4(b)**. All the phase modulators (PMs) should be replaced with other shorter (10–50 μm) and faster (40–100 GHz) PMs [12] to achieve both much lower latency and higher throughput.

5. Multibit AND circuit by cascading Ψ gates

Figure 5(a) illustrates an optimized multibit AND circuit (8-bit) in terms of latency. In this configuration, we need to use a specific Ψ gate with a 1:1:1 splitting (combining) ratio that enables truly loss-less AND operation (if $P_A = P_B = 1$, $P_{Bias} = 1$, $\Delta\Phi_{Bias} = 0$, then $P_{out} = 3$, which means no radiation loss) with phase-bit operation (when the digital input is "0" or "1," the corresponding PM modulates the relative phases $\Delta\Phi_A$ and $\Delta\Phi_B$ between π (out-of-phase) and 0 (in-phase)). Therefore, all the signal ports connect with PMs directly (no MZMs). However, this phase-bit operation is only available for the first stage because the output of the phase-shift keying operation is not *phase bit* but *amplitude bit*. For the intermediate in-phase combining, Y gates are used. At the final stage (and the first splitting stage), the Ψ gates with a 2:1:2 combining (splitting) ratio are optimal for 8-bit operation to minimize insertion loss (note that the optimal ratio for other bit-number operations is different). The combined optical signal is converted by the electrical signal and digitized through a low-latency threshold operator such as a sense amplifier [13]. It should be noted that the *BC* of the multibit AND operation degrades with the number of the cascade connection. However, the sense amplifier can operate even with a small *BC* if the absolute output intensity difference between fully matched (all the digital input are "1") and unmatched (more than one

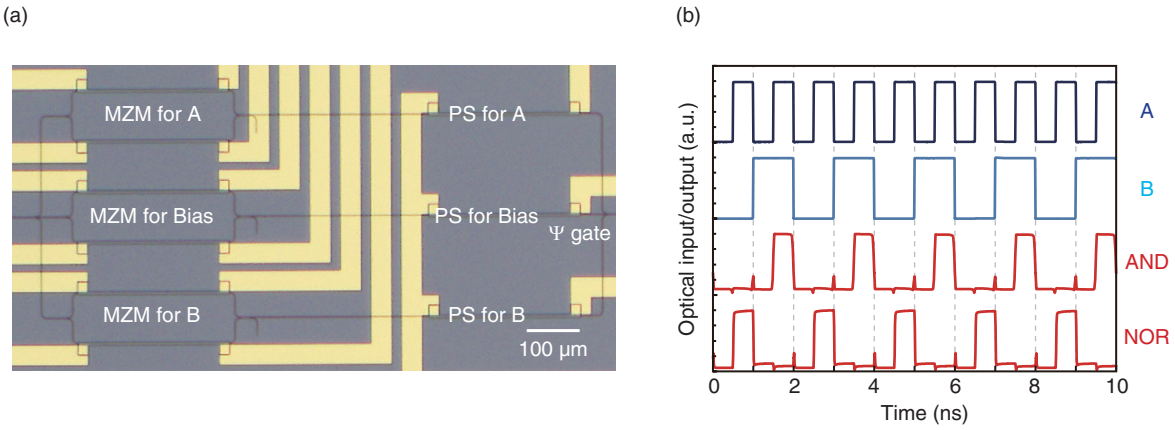

Fig. 4. Preliminary on-chip integration of a Ψ gate with three MZMs, three PSs, and a Ψ gate. (a) Optical microscope image of the whole circuit. (b) Time waveforms of optical input signals and outputs demonstrating AND and NOR logic operations.

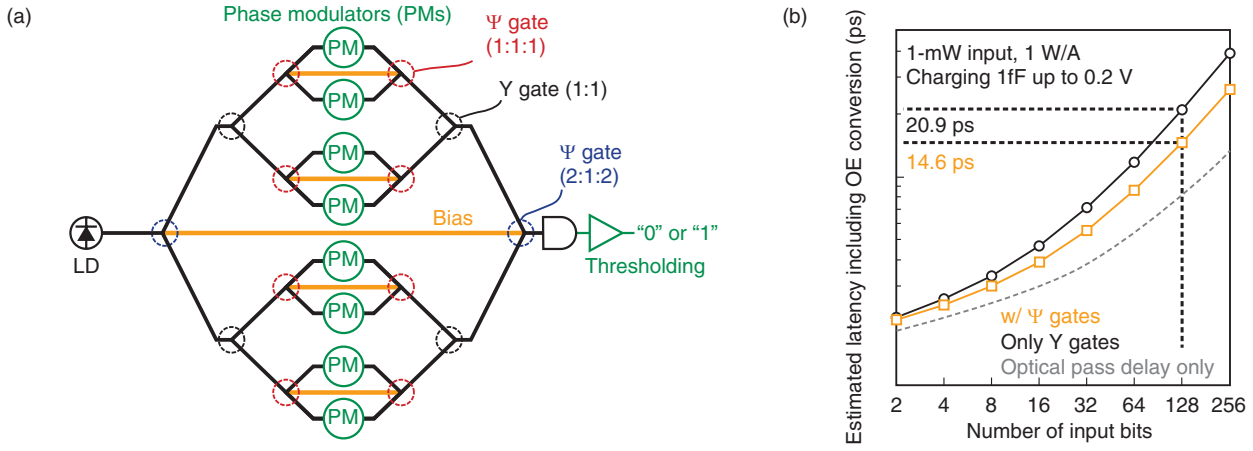

Fig. 5. Multibit AND operations using cascaded Ψ gates. (a) Schematic diagram optimized for 8-bit operation. (b) Estimated latency including photoelectric conversion against a different bit scale. In the simulation, a very small capacitance photodiode was assumed according to K. Nozaki et al. [15]. To estimate the optical pass delay, we assumed the input PM length of 200 μm, Ψ gate length of 5 μm, spacing between input PMs of 10 μm (this number is possible when we use carrier effect PMs, etc.), and bending radius of a Si waveguide of 20 μm.

input is "0" etc.) cases is large enough (typically a difference of 10–100 μW is acceptable). Therefore, the *BC* does not directly limit the feasibility of multibit AND operation. A very similar method was also proposed and demonstrated in CMOS logic circuits based on the current-race method [14]. In the current-race method, the currents from the multiple bit channels ("0" or "1" corresponds to zero or nonzero current output for each bit channel, respectively) are combined through electronic wires, and the combined current is digitized through a sense amplifier. In the case of our photonic method, the signal-combining time can be much shorter than the case of electronics, as we mentioned above. On the other hand, we have an overhead of optoelectric conversion (charging) delay due to the resistance-capacitance time constant of the used photodetector, but this could be drastically mitigated using an ultralow-capacitance (~1 fF) photodetector [15], as discussed in the next paragraph.

The computation latency of multibit AND circuits was estimated, as shown in **Fig. 5(b)**. We compared

the configurations with and without using Ψ gates and used an ultralow-capacitance photodetector with 1 fF [15]. For instance, the estimated latency for N = 128 (practical level) is ~14.6 ps. The additional charging delay of *w/ Ψ gates* always becomes half of *only Y gates* thanks to twice the *BC* (30% reduction under the same input power of 1 mW). This latency is already 10 times lower than that of the fastest CMOS 128-bit AND circuits [16]. We can also apply wavelength division multiplexing by using more than two input lasers with different wavelengths and corresponding wavelength-selective (resonator-type) electro-optic PMs, further decreasing latency. Although it is also possible to use repeaters for latency compensation, it is no longer energy efficient. The example of this multibit AND circuit application indicates that photonic processing would break the traditional trade-off between latency and energy consumption in CMOS electronics.

6. Conclusion

We experimentally demonstrated ultrashort, simple, integrable, and wavelength insensitive Si wire Ψ gates towards ultralow-latency photonic processing. From the gate length, the minimum computation latency of single logic operation is only ~30 fs, which is more than 100 times lower than that of CMOS electronics. The optical signal loss is also much lower than any other optical gates. The operation function can be switched among XOR, OR, AND, XNOR, NOR, and NAND with a single Ψ gate by tuning input conditions. We also verified the feasibility of on-chip integration for stable operation. Finally, we suggested the original configuration for multibit AND circuits by cascading Ψ and Y gates. By using this configuration, 128-bit AND operation can be carried out at 10 times lower latency than cutting-edge CMOS electronics. Latency can be further lowered by combining with multibit AND circuits and wavelength division multiplexing with a larger number of wavelength channels and by using smaller PMs based on micro rings.

We gave an example of logic operations based on linear optical gates. However, linear optical gates can perform specific vector-matrix operations (transformations) without consuming energy. The demonstrated digital-like logic operations are just a specific case of these operations. Therefore, it is expected that low-latency, low-power consumption linear-gate-based vector-matrix operations will be more crucial for photo-electronic-converged artificial-neural-network-accelerator applications [17].

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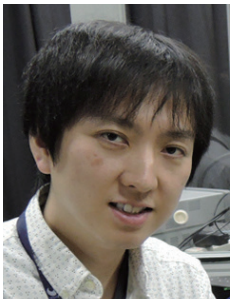

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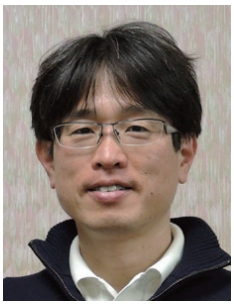

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Wearable Biological/environmental Sensor and Its Application for Smart Healthcare Services

Kei Kuwabara, Akio Tokura, Yuki Hashimoto, Yuichi Higuchi, and Hiroyoshi Togo

Abstract

Smart healthcare services using wearable biological sensors are gaining interest regarding healthy living and safe working conditions. NTT and Toray Industries, Inc. have developed a smart textile called hitoe™, which enables the measurement of biological information, such as heart rate and cardiac potential, by just wearing a shirt with hitoe electrodes. This article introduces a new sensor, which is used in combination with hitoe, that is small, has low power consumption, and enables multi-sensing of biological and environmental information. Its application for physical condition management of workers in hot environments is also introduced.

Keywords: wearable device, biological and environmental sensor, physical condition management

1. Introduction

Wearable devices with biological sensors have been used recently for monitoring lifestyle, such as exercise and sleep, to provide advice for living a healthy life. These devices are also useful to offer physical condition management services for workers, especially in summer, due to global warming. For wearable devices to sustainably contribute to living a healthy life, they need to be more natural and intuitive and blend into daily life. NTT has jointly developed the conductive textile hitoe™ through collaboration with Toray Industries, Inc. in the form of shirt-type clothing for daily biological measurements [1]. In this article, we introduce a new wearable sensor, which is used in combination with hitoe, that is small, has low power consumption, and enables multi-sensing of biological and environmental information. In Section 2, we briefly introduce wearable sensor involving hitoe and its challenges regarding natural sensing. In Section 3, we describe the features and specifications of the new sensor. In Section 4, we explain the multi-sensing technique we developed to reduce power consumption. Finally, in Section 5, we introduce an application of the sensor for physical condition management of workers in hot environments.

2. Wearable sensing technology using hitoe

The textile hitoe is a functional nanofiber material coated with the conductive polymer PEDOT-PSS[*1]. It has flexibility and breathability, and its hydrophilicity allows stable contact to the skin. As a result, biological information, such as heart rate and cardiac potential, can be measured with high sensitivity [2]. For daily monitoring of biological information, hitoe electrodes are embedded in a garment, such as the innerwear shown in **Fig. 1**. Our conventional sensor that includes analog front-end circuits, an analog-digital converter, accelerometer, central processing unit (CPU), and radio-frequency circuits for Bluetooth Low Energy communication is attached to the

*1 PEDOT-PSS: poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)

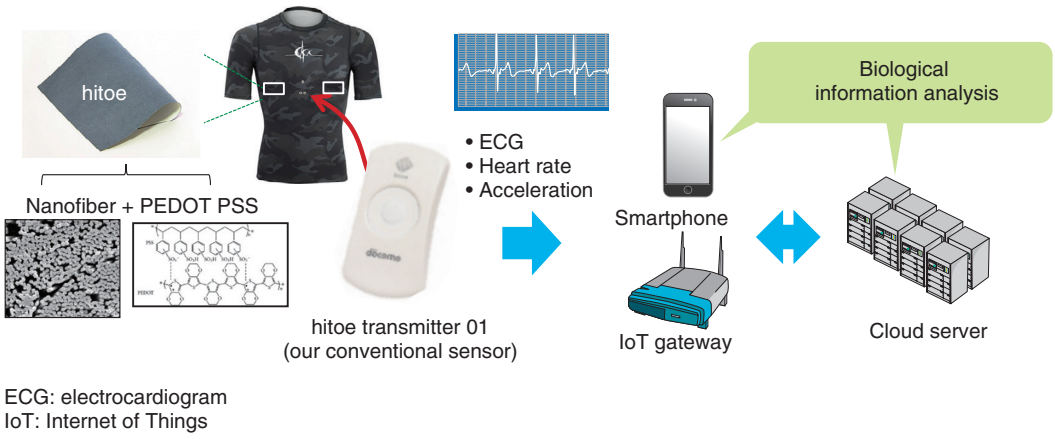


Fig. 1. Biological sensing system with hitoe™.

innerwear and connected to the hitoe electrodes via snaps on the garment. The measured data are sent to the smartphone for visualization then sent to the cloud servers for data storage and additional signal processing. This hitoe wearable sensing technology was applied for various applications such as sports, worker safety, and rehabilitation [3, 4].

To make wearable sensing technology more natural for our daily lives, miniaturization and long battery life of the sensor are required to reduce the interference with the user's movement and the frequency of battery charging. The problem that a smartphone must always be carried to collect data constantly also needs to be solved. For smart healthcare, such as physical condition management of workers in hot environments, not only biological information but also environmental information is important to evaluate the thermal stress on individuals [5]. Since conventional environmental sensors, such as wet bulb globe temperature (WBGT) heat stress monitors, are too large for natural sensing, wearable devices capable of multi-sensing of biological and environmental information are effective for such application.

3. New wearable biological/ environmental sensor

To address the above issues, we developed the wearable sensor shown in **Fig. 2** that is small (12 g), has low power consumption, and enables multi-sensing of biological and environmental information. The sensor can be attached to hitoe innerwear to measure biological information such as heart rate and cardiac potential. The sensor can also measure the environment between clothing. When outerwear is worn over the hitoe innerwear, the sensor monitors the temperature and humidity of the space between the two garments. These data are useful to assess a wearer's heat stress and comfortability. Furthermore, acceleration and angular velocity can be measured to monitor body movements. From these measurement data, the sensor can extract various feature values such as heart rate, R-R interval*2, number of steps, amount of body movement, and angle. These measurement data and the extracted feature values are transmitted to the smartphone or Internet-of-Things gateway via Bluetooth Low Energy. The extracted feature values are stored in the sensor's internal memory so that the data can be collected if the wearer does not have a smartphone during measurement. Due to the ergonomically designed housing, the sensor fits in a gap between the chest and abdomen, allowing it to be worn comfortably without obstructing movement such as bending and lying down.

4. Multi-sensing technique for low power operation

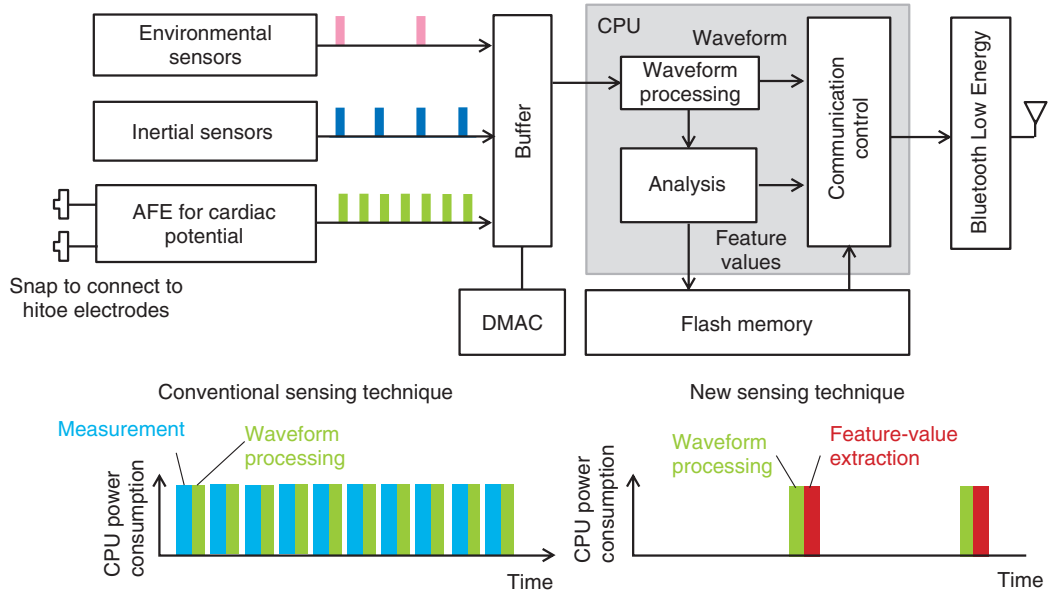
When various data are continuously measured, analyzed, and transmitted, the CPU load and power consumption increase. As a result, frequent charging is required due to shortened operation time or a large battery is required to maintain operation time. To overcome these problems, our sensor uses a multi-sensing technique we developed to reduce power

*2 R-R interval: The time between the peaks of two successive R waves in electrocardiogram waveforms.

Appearance	
Size	64 × 36 × 9 mm
Weight	12 g
Measurement data	Cardiac potential, temperature and humidity between clothes, acceleration, angular velocity
Extracted feature values	Heart rate, R-R interval, number of steps, amount of body movement, angle
Memory	Storage of extracted feature values

LED: light emitting diode

Fig. 2. Specifications of new wearable biological/environmental sensor.



AFE: analog front-end
DMAC: direct memory access controller

Fig. 3. Circuit configuration and flow of low-power multi-sensing technique.

consumption. **Figure 3** shows the circuit configuration and flow of this technique. By effectively using a direct memory access controller, various data are measured and accumulated in a buffer while the CPU is sleeping. After a certain amount of data has been accumulated, the CPU is activated only for a short time to perform waveform processing and feature-value extraction.

Table 1. Operational modes of wearable biological/environmental sensor.

Mode	Standard	High performance	Low power
Cardiac potential waveform	200 Hz	1 kHz	–
Inertial sensor	Acceleration	Acceleration & angular velocity	–
Feature values*	Good	Good	Good
Battery life	Good	Neutral	Very good

* Feature values include heart rate, R-R interval, temperature, humidity, number of steps, amount of body movement, and angle.

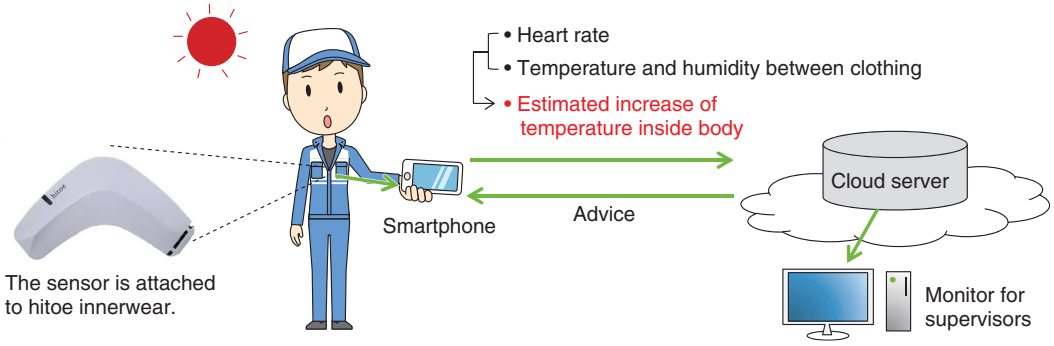


Fig. 4. Prototype system for physical condition management of workers in hot environments.

Our biological/environmental sensor has the three operating modes shown in **Table 1** to meet different requirements, e.g., the necessity of waveform and angular velocity, and battery life depending on the application. In standard mode, the transmission of the cardiac potential waveform at a sampling rate of 200 Hz, acceleration waveform, and extracted feature values is enabled. In high performance mode, the sampling rate of the cardiac potential waveform is improved to 1 kHz, and the angular velocity measurement is enabled. In low power mode, the battery life is extended by stopping the waveform transmission.

By reducing the CPU load, this sensor in standard mode operates at about 30% the power consumption of our conventional sensor but with additional measurement and analysis functions. In low power mode, the power consumption is further reduced to about 15% that of the conventional sensor. As a result, the new sensor is about half the size of the conventional one by using a smaller battery, and more than 100 hours of operation is possible in low power mode.

5. Application to physical condition management of workers in hot environments

As an application of the wearable biological/environmental sensor, we are developing a physical condition management system for workers in hot environments, as shown in **Fig. 4**.

While conventional systems using WBGT sensors are effective in providing an indication of heat stress in certain areas, the environment may change significantly depending on the location such as indoors or outdoors or in sunlight or shade. The clothing and activities also affect the heat stress on individuals. In a prototype of our system, our wearable biological/environment sensor is attached to hitoe innerwear to measure heart rate and the temperature and humidity between the innerwear and outerwear. To evaluate the heat stress on an individual, the heat exchange between the environment and human body is calculated from the measured data, and the heat stored in the body is estimated. If the temperature is expected to rise, workers and supervisors receive advice such as drink more water and take breaks. We are collaborating with universities including Nagoya Institute of

Technology to improve and verify the accuracy of the heat estimation through experiments in an artificial weather control room. The field trials at the construction sites of NTT Group companies are scheduled this summer to evaluate the effectiveness of the system. We will work to create smart healthcare services that use wearable biological/environmental sensors through these trials.

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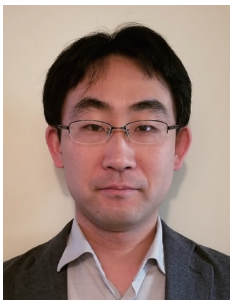

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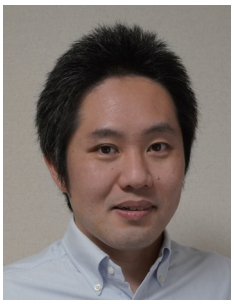

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Recent Activities of QoE-related Standardization in ITU-T SG12

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Abstract

This article introduces recent standardization activities related to the evaluation of the quality of experience (QoE) of speech and video services, focusing on the activities of ITU-T SG12 (International Telecommunication Union - Telecommunication Standardization Sector, Study Group 12), which is responsible for standardization work on performance, quality of service, and QoE.

Keywords: adaptive bitrate streaming, crowdsourcing, gaming, quality of experience, virtual reality

1. Introduction

The International Telecommunication Union - Telecommunication Standardization Sector, Study Group 12 (ITU-T SG12) is a lead study group on network performance and quality of service (QoS) and quality of experience (QoE). In January 2017, SG12 was restructured by incorporating two questions on quality assessment, which had been studied in SG9. ITU-T SG12 is the leader in the worldwide standardization of speech and video quality evaluation, taking into account achievements in regional standardization bodies such as ETSI (European Telecommunications Standards Institute) and ATIS (Alliance for Telecommunications Industry Solutions). Standardization work on network performance parameters is carried out in various standardization organizations and all these organizations have confirmed that their work matches that of SG12.

2. Full-band and super-wideband E-model (G.107.2)

ITU-T standardized a quality-planning tool for telephony services as Recommendation G.107, which is also called the E-model. The output of the E-model is the R-value as a transmission rating scale. Q.15/12 (Parametric and E-model-based planning, prediction and monitoring of conversational speech quality) extended the scope of G.107 so that it can cover super-wideband (50–14,000 Hz) and full-band (20–20,000 Hz) speech communication services and standardized Recommendation G.107.2. This enables us to calculate the quality of super-wideband and full-band speech encoded by EVS (Enhanced Voice Services).

3. Quality-estimation model for adaptive bitrate streaming (P.1203 and P.1204)

An important application of QoE estimation methods is in-service non-intrusive quality monitoring. For such a scenario, parametric quality models, which calculate QoE on the basis of packet-header information or metadata such as bitrate, should be developed due to the limited computational resources of end-clients.

Q.14/12 (Development of models and tools for multimedia quality assessment of packet-based video services) has been working on models for adaptive bitrate streaming, namely P.1203 and P.1204. P.1203 can be used to estimate the quality of adaptive bitrate steaming with high-definition resolution video encoded by H.264/AVC (Advanced Video Coding). The P.1203 model consists of video- and audio-quality-estimation modules (P.1203.1 and P.1203.2) and an integration module (P.1203.3). The video- and audio-quality-estimation modules calculate video and audio quality per second, and the integration module takes video and audio quality and stalling information

to calculate overall audiovisual quality. In addition, the video-quality-estimation module (P.1203.1) has four modes. The module takes metadata such as bitrate, framerate, and resolution in mode 0; frame-level information in addition to the input of mode 0 in mode 1; 2% of bitstream information in mode 2; and full bitstream information in mode 3.

Recently, 4K resolution videos encoded by H.265/HEVC (High Efficiency Video Coding) and VP9 have become popular. Therefore, in P.1204, Q.14/12 extended the scope of P.1203 so that it can cover these applications. In other words, the extension of the video-quality-estimation module has been studied. In P.1204, there are five models: a mode-0 model (P.1204.1), mode-1 model (P.1204.2), mode-3 model (P.1204.3), full-reference and reduced-reference pixel-based model (P.1204.4), and hybrid model (P.1204.5). P.1204.3, P.1204.4, and P.1204.5 have been standardized, but P.1204.1 and P.1204.2 are still being studied.

4. QoE-influencing factors and subjective evaluation for 360-degree video (G.1035 and P.360-VR)

As the fifth-generation mobile communication system (5G) is being launched, higher-speed and lower-latency video streaming services are expected. Since virtual reality (VR) is expected as one of the most promising services, Q.13/12 (Quality of experience (QoE), quality of service (QoS) and performance requirements and assessment methods for multimedia) has been studying subjective evaluation methodology to assess the quality of VR services.

In VR video streaming services, many users become nauseous due to motion sickness while watching VR video. Therefore, QoE-influencing factors for VR services are defined in detail in G.1035.

A new subjective evaluation methodology (P.360-VR) has been studied because a head-mounted display is worn to watch VR video streaming services, in contrast to regular two-dimensional video streaming services. A subjective evaluation methodology needs to be developed for VR video streaming services on the basis of the results of stability and reliability in many experiments. In addition, detailed procedures need to be described in the recommendation. In these tests, SG12 relies on the test results provided by VQEG (Video Quality Experts Group), and many tests have already been conducted. However, statistical analysis has not been completed. After the statistical analysis is conducted, the final draft of P.360-VR will be submitted in September 2020.

5. QoE-influencing factors, subjective evaluation, and opinion model for gaming applications (G.1032, P.809, and G.1072)

Since gaming applications have spread rapidly, their QoE-influencing factors (G.1032) need to be identified, and a subjective assessment methodology (P.809) and quality-estimation model (G.1072) for them need to be developed. Like VR services, gaming applications have many QoE-influencing factors, so video, audio, and latency-related factors are described in detail in G.1032.

A subjective evaluation methodology for gaming applications is standardized in Recommendation P.809. In general, the five-point ACR (absolute category rating) is widely used in telecommunication. However, the seven-point continuous scale defined in P.851 is recommended because gaming applications have many QoE-influencing factors.

Like the E-model for telephony services, a quality-planning tool for gaming applications has been studied and standardized as Recommendation G.1072. In this recommendation, mathematical equations and parameters are defined. In other words, special software is not necessary. Therefore, this enables network operators and application developers to easily use the model, which takes parameters such as bitrate as input and calculates the quality of gaming applications.

6. Subjective evaluation with a crowdsourcing approach (P.808, P.CROWDV, P.CROWDG)

Subjective evaluation testing is generally conducted using special equipment and on the basis of expertise. However, to obtain quality from the actual services and obtain much high-quality data, subjective evaluation with a crowdsourcing approach has been studied and standardized in Recommendation P.808, which is used for evaluating speech quality. In addition, like speech quality, subjective evaluation with a crowdsourcing approach has been studied for video streaming and gaming applications because the demand to evaluate the quality of their applications with a crowdsourcing approach is increasing.

7. 2021–2024 study period

The structure of SG12 in the 2021–2024 study period has been discussed. Although the current

structure will basically be maintained, several questions will be closed and several others will be opened. Maintenance of recommendations under the responsibility of Q.3/12 (Speech transmission and audio characteristics of communication terminals for fixed circuit-switched, mobile and packet-switched Internet protocol (IP) networks) will be transferred to Q.5/12 (Telephonometric methodologies for handset and headset terminals) and Q.6/12 (Analysis methods using complex measurement signals including their application for speech and audio enhancement techniques). Q.18/12 (Measurement and control of the end-to-end quality of service (QoS) for advanced television technologies, from image acquisition to rendering, in contribution, primary distribution and secondary distribution networks) was closed because of a lack of contributions. However, maintenance of recommendations under the responsibility of Q.18/12 was transferred to Q.19/12 (Objective and subjective methods for evaluating perceptual audiovisual quality in multimedia and television services) during the 2017–2020 study period. In addition, a new question will be launched to study digital financial services, which were studied under Q.13/12

8. Outlook

This article described subjective assessment and quality-estimation models for speech, video streaming, and gaming applications. VR video streaming services and subjective evaluation with a crowdsourcing approach have been studied. Recently, SG12 has studied, for example, the analysis of quality-impairment factors and quality-estimation models using artificial intelligence technologies. Since many new services, such as telemedicine, are expected to be launched in the 5G era, more complicated issues related to QoS and QoE need to be addressed, for example, the demand of QoS and QoE planning and management. Therefore, it is important to investigate the recent activities of SG12.

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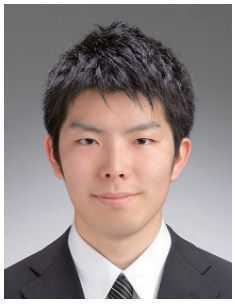

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Quick and Automatic Solution of Electromagnetic Disturbance by Using the Intelligent Noise Filter

Technical Assistance and Support Center, NTT EAST

Abstract

This article introduces the *intelligent noise filter* developed by Technical Assistance and Support Center, NTT EAST. The intelligent noise filter can quickly and easily suppress an electromagnetic disturbance that may cause problems in telecommunication networks. This is the sixtieth article in a series on telecommunication technologies.

Keywords: noise filter, electromagnetic disturbance, frequency detection

1. Introduction

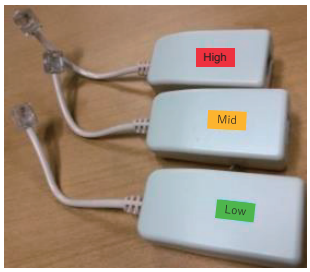
An electromagnetic disturbance generated from malfunctioning electric/electronic equipment may affect the telecommunication signals being transmitted on a copper cable. An electromagnetic disturbance may cause problems in telecommunication networks such as audible noise in analog telephones, connection loss or quality degradation of Asymmetric Digital Subscriber Lines (ADSLs), and transmission errors on Integrated Services Digital Network (ISDN) lines. To solve these problems, it is necessary to identify the source of the electromagnetic disturbance and remove it. However, this is difficult to do in many cases in the field. An electromagnetic interference suppression (EMI) filter is useful for removing such disturbance when the source of the disturbance cannot be identified. However, to use an EMI filter, service personnel need to use special techniques, such as measuring the frequency of the disturbance and selecting the appropriate EMI filter. Moreover, if an electromagnetic disturbance randomly appears in the cable, it takes time to determine the characteristics of the disturbance. Therefore, Technical Assistance and Support Center (TASC), NTT EAST, developed a new measurement tool for removing electromagnetic disturbance last year. The tool, called *intelligent noise filter*, can be used to automatically measure the frequency of the electromagnetic disturbance and automatically insert the appropriate EMI filter built into the device into the copper cable [1]. This article introduces key features of and how to use the intelligent noise filter.

2. Key features of the intelligent noise filter

There are many types of EMI filters according to the frequency range and telecommunication services. Therefore, the intelligent noise filter is used to measure the frequency range of the electromagnetic disturbance, making it possible to select the most appropriate EMI filter.

A photograph of the intelligent noise filter is shown in **Fig. 1(a)**. It is 45 mm in height, 175 mm in width, and 125 mm in depth and weighs about 500 g. Since it can operate for about 200 hours on four AA alkaline batteries, its power supply at the installation site is not a matter of concern. We also developed three types of EMI filters for permanent measures, as shown in **Fig. 1(b)**. Each filter has the same attenuation

(a) Intelligent noise filter (with built-in EMI filters)



(b) Newly developed EMI filters

Fig. 1. (a) Intelligent noise filter and (b) newly developed EMI filters.

characteristic in accordance with the frequency range specified by the main unit of the intelligent noise filter. When the frequency range of the electromagnetic disturbance is determined using the intelligent noise filter, we can replace the built-in EMI filter with the appropriate newly developed EMI filter.

2.1 Noise measurement and filter specifications

The specifications of the intelligent noise filter and the newly developed EMI filters are listed in **Table 1**. The intelligent noise filter detects and suppresses noise. To detect noise, the intelligent noise filter measures the frequency range of an electromagnetic disturbance between 2 kHz to 12 MHz. This frequency range is also divided into three bands: 2 to 15 kHz (Low), 15 to 300 kHz (Mid), and 0.3 to 12 MHz (High). To suppress noise, the built-in EMI filters attenuate noise in accordance with three frequency bands.

The newly developed EMI filters have the same specifications as the built-in EMI filters in terms of frequency range and attenuation level. Common mode attenuation, which indicates how much electromagnetic disturbance can be suppressed, is 40 dB or more in any frequency range. Differential mode attenuation, which indicates the attenuation of the telecommunication signal, is 1.5 dB or less when they are installed in an analog line and 3 dB or less when installed in a digital line.

Table 1. Specifications of the intelligent noise filter and newly developed EMI filters.

Item	Performance	
Frequency range	Low	2 k–15 kHz
	Mid	15 k–300 kHz
	High	300 k–12 MHz
Common mode attenuation	Low	40 dB or more
	Mid	40 dB or more
	High	40 dB or more
Differential mode attenuation	Low	1.5 dB or less (600 Ω), 3 dB or less (110 Ω)
	Mid	1.5 dB or less (600 Ω), 3 dB or less (110 Ω)
	High	1.5 dB or less (600 Ω), 3 dB or less (110 Ω)

Both the built-in EMI filters and the newly developed EMI filters effectively suppress electromagnetic disturbance while minimizing its impact on communication quality.

2.2 Noise detection

The intelligent noise filter automatically detects the frequency range of an electromagnetic disturbance and turns on an indicator corresponding to the detected frequency range (Low, Mid, or High). Electromagnetic disturbance voltage of –20 dBV (0.1 V) or higher can be detected, and it is possible to adjust the detection voltage level from –10 dBV (0.3 V) to –40 dBV (0.01 V) by adjusting the detection sensitivity volume.

2.3 EMI-filter-installation mode

The intelligent noise filter has two modes, i.e., manual and automatic, to install one of the built-in EMI filters according to the detected frequency range.

Manual mode

The appropriate built-in EMI filter can be applied by pressing the button corresponding to the detected disturbance-frequency range indicated by the illuminated indicator.

Automatic mode

When an electromagnetic disturbance is detected, the built-in EMI filter corresponding to that frequency range is automatically applied. The application flow of the corresponding filter when automatic

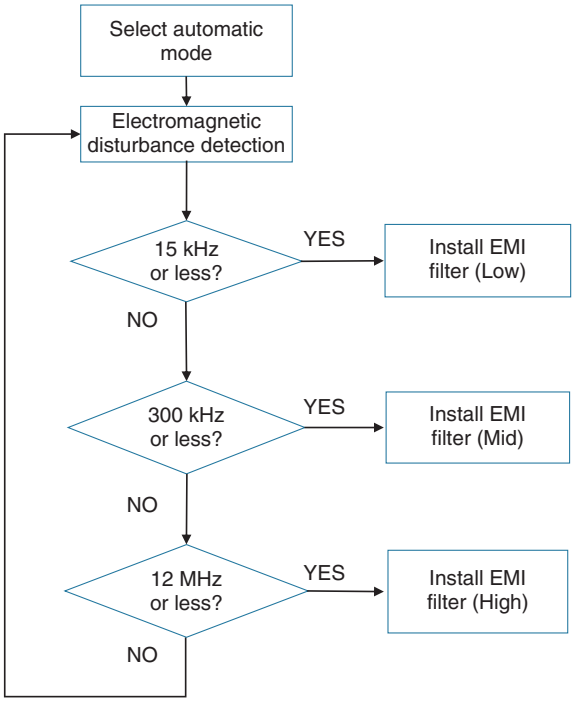


Fig. 2. Flow of applying built-in EMI filter when automatic mode is set.

mode is set is shown in **Fig. 2**.

2.4 Using the intelligent noise filter

The intelligent noise filter is used according to the following procedure.

(1) Install the intelligent noise filter on a copper cable, on which audible noise, transmission error, or other problems caused by electromagnetic disturbance have occurred, and switch its power supply on.

(2) When an electromagnetic disturbance occurs, the intelligent noise filter automatically detects it, and the indicator corresponding to the detected frequency range is illuminated. In manual mode, a service personnel presses the button corresponding to the detected frequency range to apply the appropriate built-in EMI filter (Low, Mid, or High). In automatic mode, the intelligent noise filter automatically applies the built-in EMI filter that corresponds to the frequency range of the detected noise.

(3) After confirming the effect of the built-in EMI filter, that filter is replaced with the corresponding newly developed EMI filter (Low, Mid, or High) for permanent measures.

3. Countermeasures using the intelligent noise filter

Practical countermeasures using the intelligent noise filter are described in this section.

3.1 Countermeasure against telecommunication problems occurring on an ADSL

A customer who uses an ADSL reported that a link down of the ADSL frequently occurs. Although local service personnel took countermeasures such as replacing the ADSL modem, the link down could not be resolved. Therefore, TASC investigated the electromagnetic disturbance and implemented a countermeasure by using the intelligent noise filter (**Fig. 3**).

First, when the intelligent noise filter was installed between the ADSL modem and splitter, the Mid indicator was illuminated (**Fig. 4(a)**). Then, when the button of the Mid filter was pressed, i.e., the built-in EMI filter (Mid) was applied, the link down of the ADSL was resolved (**Fig. 4(b)**). Finally, TASC replaced the built-in EMI filter (Mid) with the newly developed EMI filter (Mid) for permanent measures.

The transmission rate of the ADSL was improved by installing the appropriate newly developed EMI filter. The results of the measured bit maps before and

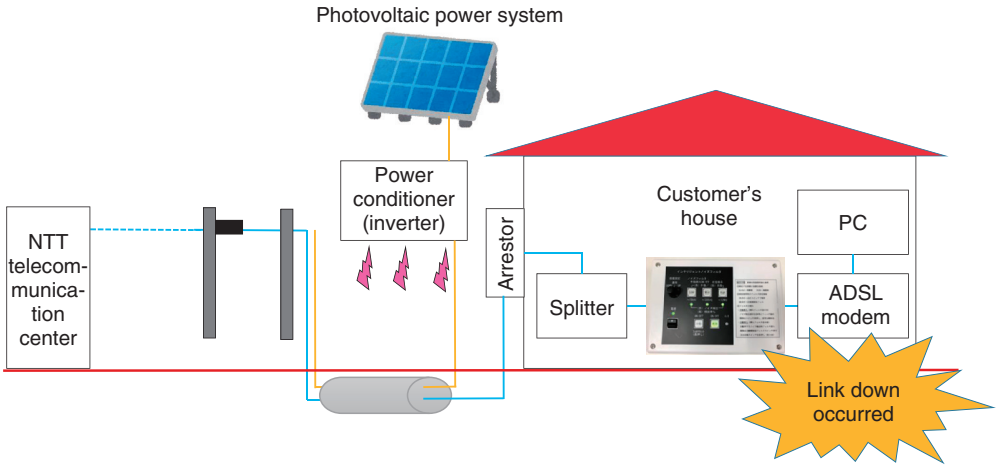


Fig. 3. Configuration of customer's equipment and telecommunication network.

(a) When electromagnetic disturbance is detected

(b) When the built-in EMI filter is applied

Fig. 4. Operation screen of intelligent noise filter.

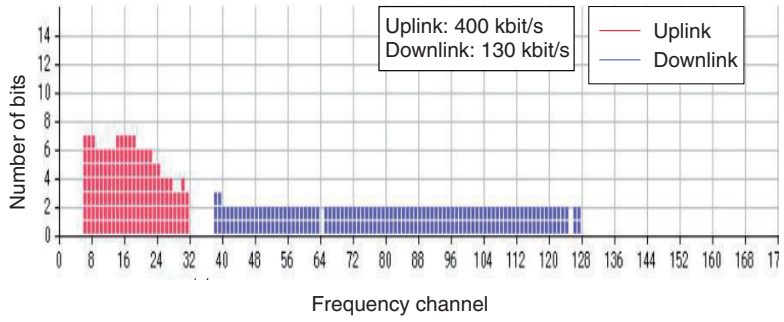
after installing the filter are shown in **Fig. 5**. Transmission rate increased from 400 kbit/s to 1 Mbit/s on the uplink and from 130 kbit/s to 3 Mbit/s on the downlink.

TASC also investigated the source of the electromagnetic disturbance and found that it was being generated by the power conditioner of a photovoltaic power system installed near the customer's house. The noise was being transmitted through the power line cable and induced in the telecommunication cable, which was laid out parallel to it, thereby affecting the ADSL signal.

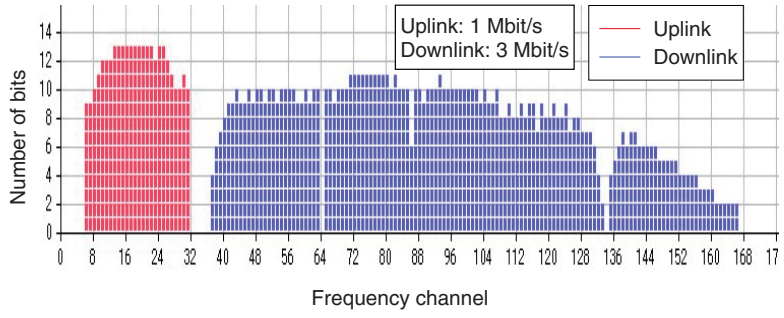
3.2 Countermeasure against audible noise occasionally heard on 3.4k leased line

A customer who uses a 3.4k leased line between two locations reported an audible noise (a "bee" sound) mixed into the telephone signal at an occurrence frequency of once a week. Local service personnel had difficulty in responding to the problem because the audible noise was not generated when they visited the customer's house. Therefore, TASC investigated the noise and implemented a countermeasure using the intelligent noise filter (**Fig. 6**).

The intelligent noise filter was installed between the leased-line terminal and arrester in the customer's house. Since the disturbance occurred sporadically, the automatic-mode button was pressed to detect and monitor the disturbance for one week (**Fig. 7(a)**). After that week, the customer informed us that the audible noise no longer occurred, so when the service personnel visited, the Low indicator was illuminated and the built-in EMI filter (Low) was applied automatically (**Fig. 7(b)**). Subsequently, that filter was replaced with the newly developed EMI filter (Low). It was found that low-frequency noise entered the power line cable. Thus, the source of the disturbance was determined as the power-supply unit or the power-supply source that starts up irregularly.

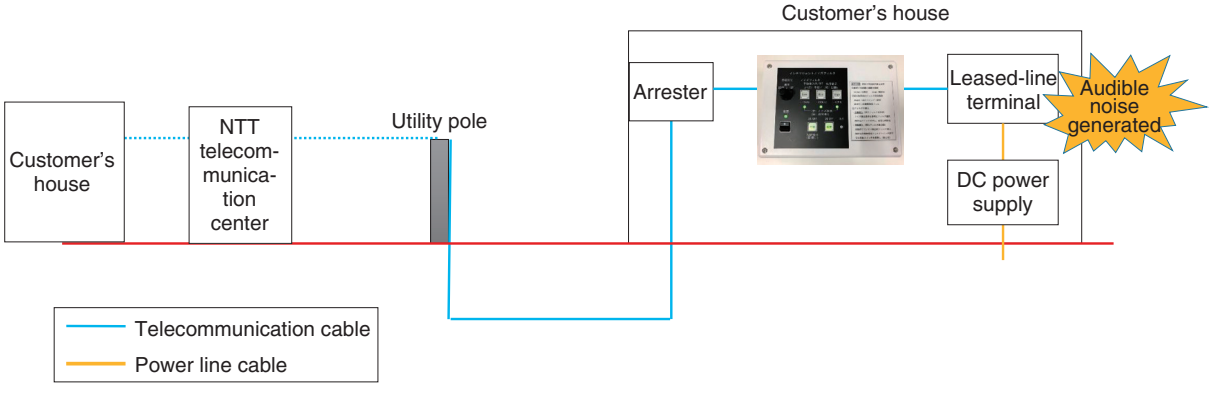


(a) Before installing EMI filter



(b) After installing EMI filter

Fig. 5. Bitmaps before and after installation of the newly developed EMI filter.



DC: direct current

Fig. 6. Configuration of customer's equipment and telecommunication network.

4. Concluding remarks

The key features of the intelligent noise filter developed by TASC were introduced and actual countermeasures against telecommunication problems caused by electromagnetic disturbance were described. From these countermeasures, using the intelligent noise filter makes it possible to recover from telecommunication problems caused by electromagnetic disturbance without the need for specialist

(a) When the automatic mode button is pressed

(b) When the built-in EMI filter (Low) is automatically applied

Fig. 7. Operation screen of intelligent noise filter (automatic mode).

skills; accordingly, it is expected to alleviate the implementation of countermeasures against such problems.

To reduce telecommunication problems caused by electromagnetic disturbance, radio, induction, lightning, etc., and improve the reliability of telecommunication services, the EMC Engineering Group in TASC will continue to actively engage in technical cooperation and development and disseminate their technologies through activities such as technology seminars.

Reference

[1] "Development of Intelligent Noise Filter for Skill-less Electromagnetic Disturbance Countermeasures," NTT Technical Journal, Vol. 30, No. 4, pp. 61–63, Apr. 2018 (in Japanese).

External Awards

Certificate of Appreciation
Winner: Seishi Takamura, NTT Media Intelligence Laboratories
Date: June 12, 2020
Organization: IEEE Region 10 Symposium (TENSYMP2020) Organizing Committee

For his contribution to the quality of the symposium by delivering keynote speech titled "Latest Advances in Video Coding Technology for Immersive Visual Communications."

Excellent Oral Presentation
Winner: Hideaki Kimata, NTT Media Intelligence Laboratories
Date: July 6, 2020
Organization: The 4th International Conference on Graphics and Signal Processing (ICGSP 2020)

For "Hierarchical and Compact Bitmap Based Data Structure of Human Dynamics Data for Visualization."
Published as: H. Kimata, W. Xiaojun, R. Tanida, "Hierarchical and Compact Bitmap Based Data Structure of Human Dynamics Data for Visualization," ICGSP 2020, June 2020 (online).

IEICE Communications Express Top Downloaded Letter Award in June 2020
Winners: Yuki Arikawa, Hiroyuki Uzawa, Takeshi Sakamoto, Satoshi Shigematsu, and Shunji Kimura, NTT Device Innovation Center
Date: July 17, 2020
Organization: The Institute of Electronics, Information and Communication Engineers (IEICE) Communications Express

For "High-speed Radio-resource Scheduler with Hardware Accelerator for Fifth Generation Mobile Communications Systems."
Published as: Y. Arikawa, H. Uzawa, T. Sakamoto, S. Shigematsu, and S. Kimura, "High-speed Radio-resource Scheduler with Hardware Accelerator for Fifth Generation Mobile Communications Systems," IEICE Commun. Exp., Vol. 6, No. 5, pp. 236–241, 2017.

Encouraging Award
Winner: Ryo Igarashi, NTT Access Network Service Systems Laboratories
Date: September 11, 2020
Organization: IEICE Technical Committee on Communication Systems

For "Reach Extension of 10G-EPON Upstream Transmission using Distributed Raman Amplification."
Published as: R. Igarashi, T. Kanai, M. Fujiwara, H. Suzuki, J. Kani, J. Terada, "Reach Extension of 10G-EPON Upstream Transmission using Distributed Raman Amplification," IEICE Tech. Rep., Vol. 119, No. 365, CS2019-94, pp. 33–38, Jan. 2020.

Distinguished Contributions Award
Winner: Miyuki Imada, NTT Service Evolution Laboratories
Date: September 15, 2020
Organization: IEICE Communications Society

For her contribution to the IEICE Communications Society as a secretary of planning, the Council of Technical Committee Representatives.

Papers Published in Technical Journals and Conference Proceedings

Arena-style Immersive Live Experience (ILE) Services and Systems: Highly Realistic Sensations for Everyone in the World
J. Nagao, K. Tanaka, and H. Imanaka
ITU Journal: ICT Discoveries, Vol. 3, No. 1, pp. 33–41, May 2020.

Immersive live experiences (ILEs) enable audiences at remote sites to feel real-time highly realistic sensations, as if they were at the event site. This article discusses the key functionalities of an implementation of ILE services called "Kirari! for Arenas" as a use case of arena-style ILE and its technical elements developed by NTT laboratories. The key functionalities are object extraction from an arbitrary background, object tracking with depth sensors, low-latency synchronized data transport, and four-sided pseudo-3D image presentation with depth expression. This article also provides evaluations on the experience of Kirari! for Arena audiences, as well as its conformance to International Telecommunication Union, Telecommunication Standardization Sector (ITU-T) standards for ILEs.

Quanum Remote Sensing under the Effect of Dephasing
H. Okane, H. Hakoshima, Y. Takeuchi, Y. Seki, and Y. Matsuzaki
arXiv:2007.15903 [quant-ph], August 2020.

Quantum remote sensing (QRS) is a scheme to add security about

the measurement results of a qubit-based sensor. A client delegates a measurement task to a remote server that has a quantum sensor, and eavesdropper (Eve) steals every classical information stored in the server side. By using quantum properties, the QRS provides an asymmetricity about the information gain where the client gets more information about the sensing results than Eve. However, quantum states are fragile against decoherence, and so it is not clear whether such a QRS is practically useful under the effect of realistic noise. Here, we investigate the performance of the QRS with dephasing during the interaction with the target fields. In the QRS, the client and server need to share a Bell pair, and an imperfection of the Bell pair leads to a state preparation error in a systematic way on the server side for the sensing. We consider the effect of both dephasing and state preparation error. The uncertainty of the client side decreases with the square root of the repetition number M for small M, which is the same scaling as the standard quantum metrology. On the other hand, for large M, the state preparation error becomes as relevant as the dephasing, and the uncertainty decreases logarithmically with M. We compare the information gain between the client and Eve. This leads us to obtain the conditions for the asymmetric gain to be maintained even under the effect of dephasing.

Trusted Center Verification Model and Classical Channel Remote State Preparation

T. Morimae and Y. Takeuchi

arXiv:2008.05033 [quant-ph], August 2020.

The classical channel remote state preparation (ccRSP) is an important two-party primitive in quantum cryptography. Alice (classical polynomial-time) and Bob (quantum polynomial-time) exchange polynomial rounds of classical messages, and Bob finally gets random single-qubit states while Alice finally gets classical descriptions of the states. In [T. Morimae, arXiv:2003.10712], an information-theoretically-sound non-interactive protocol for the verification of quantum computing was proposed. The verifier of the protocol is classical, but the trusted center is assumed that sends random single-qubit states to the prover and their classical descriptions to the verifier. If the trusted center can be replaced with a ccRSP protocol while keeping the information-theoretical soundness, an information-theoretically-sound classical verification of quantum computing is possible, which solves the long-standing open problem. In this paper, we show that it is not the case unless bounded-error quantum polynomial time (BQP) is contained in MA (the Merlin–Arthur protocol). We also consider a general verification protocol where the verifier or the trusted center first sends quantum states to the prover, and then the prover and the verifier exchange a constant round of classical messages. We show that the first quantum message transmission cannot be replaced with an (even approximate) ccRSP protocol while keeping the information-theoretical soundness unless BQP is contained in AM (the Arthur–Merlin protocol). We finally study the verification with the computational soundness. We show that if a ccRSP protocol satisfies a certain condition even against any quantum polynomial-time malicious prover, the replacement of the trusted center with the ccRSP protocol realizes a computationally-sound classical verification of quantum computing. The condition is weaker than the verifiability of the ccRSP. At this moment, however, there is no known ccRSP protocol that satisfies the condition. If a simple construction of such a ccRSP protocol is found, the combination of it with the trusted center verification model provides another simpler and modular proof of the Mahadev's result.
