H.264/AVC Codec LSI Configuration Technology and Application to IP Retransmission Services

Koyo Nitta†, Hiroe Iwasaki, and Jiro Naganuma

Abstract

NTT Cyber Space Laboratories has developed a codec LSI called SARA that conforms to H.264/AVC, the latest video coding standard. Proprietary architecture configuration technology enables SARA to be applied to codecs for professional broadcasting use. Transcoder equipment using SARA can be used for IP retransmission (retransmission of digital TV programs over an Internet protocol network) services on the Next Generation Network (NGN).

1. From MPEG-2 to H.264/AVC

The MPEG-2 standard used for terrestrial and broadcast satellite digital broadcasts is one of the most widely used video coding standards today, but the movement toward high-definition video in recent years has prompted the standardization of H.264/AVC (H.264) video coding, which can achieve about twice the coding efficiency of MPEG-2. From this background, we have developed an H.264 codec (coder/decoder) large-scale integrated circuit (LSI) called SARA (super advanced realtime codec architecture) [1].

NTT has been involved in the development of video codec LSIs and equipment for over ten years (**Fig. 1**). Our single-chip high-definition television (HDTV) MPEG-2 codec LSI called VASA developed in 2002 has been deployed successfully in many broadcast studios for transmitting video material in digital terrestrial broadcasting [2]. The SARA chip, which applies technology developed for VASA, is a video codec LSI for professional broadcasting use conforming to H.264/AVC, the latest video coding standard [3].

† NTT Cyber Space Laboratories
Yokosuka-shi, 239-0847 Japan

2. Requirements for professional broadcasting use

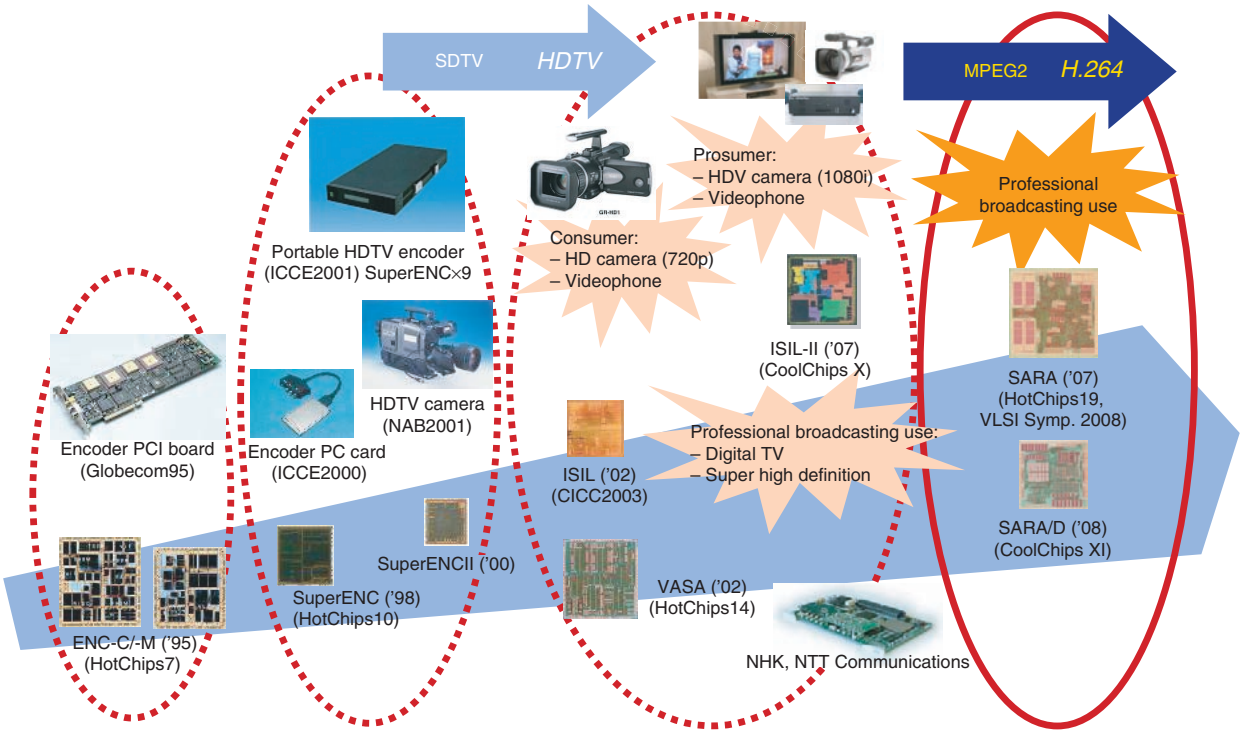
Video transmission by broadcast facilities has three main requirements:

(1) Material transmission between key studios: low delay, high quality (4:2:2 format)
(2) Relay transmission between shooting location and studio: low delay, compact configuration
(3) Delivery from broadcast studio to customers: high compression, high quality (4:2:0 format)

In short, there are various requirements depending on the transmission format, and the codec LSI must have sufficient performance to cover all of them. In particular, it must exhibit high performance for both delay and image quality, for which there is normally a tradeoff. Furthermore, in addition to the usual 4:2:0 chroma format, it must also support the 4:2:2 chroma format that contains twice the chroma information.

3. SARA coding architecture

The coding architecture of SARA is shown in **Fig. 2**. This is a multiprocessor system-on-a-chip consisting of three RISC (reduced instruction set computer) processors, dedicated hardware engines, and embedded DRAM (dynamic random access memory). The coding core is divided into two sections: the M-CORE that performs motion estimation and compensation and the C-CORE that performs arithmetic



HDV: format for recording and playing back high-definition video
PC: personal computer
PCI: peripheral component interconnect
Prosumer: professional/consumer

Fig. 1. Past video codec LSIs and equipment and SARA.

coding and rate control. The chosen configuration gives each of these sections a RISC processor to enable detailed control of its dedicated hardware engine.

The highly functional pre-analysis section (IR, MBP, RIT) analyzes statistical information in the input video and prior coding information (if present). These functions enable high-compression, high-quality video to be achieved.

While standard definition (SD) video coding is achieved with one SARA chip, HD video coding is achieved by parallel coding using multiple chips, that is, by screen-partitioned parallel coding. This approach secures sufficient processing time and high image quality for each of the partitioned areas while minimizing delay.

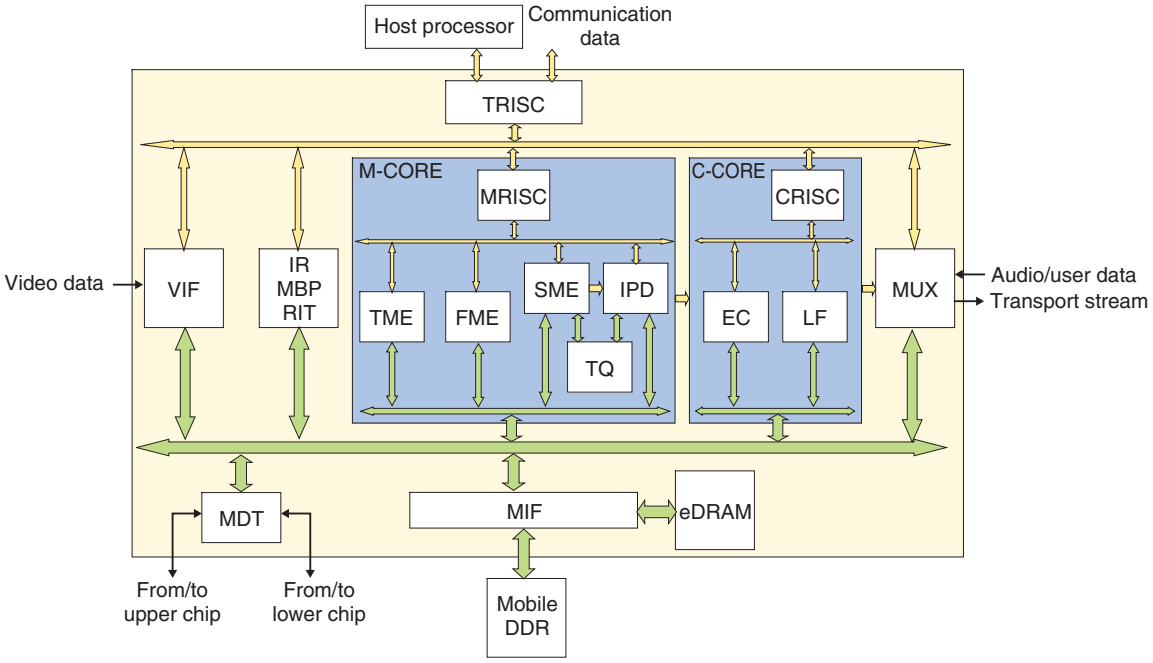
The problem of the greater memory bandwidth needed to support the 4:2:2 format is solved by using eDRAM and proprietary memory mapping technology.

4. Modules and codec equipment

SARA not only supports HD encoding and decoding, but can be implemented in a compact, postcard-size module. In particular, the encoding module uses mobile DDR SDRAM (double-data-rate synchronous DRAM), which is ideal for small electronic devices, to enable multiple SARA LSIs and external memory to be arranged densely. This module design approach not only allows for compact equipment but also enables encoding/decoding modules to be flexibly combined to produce MPEG-2-to-H.264 coding-conversion equipment (transcoders) and highly functional codec equipment like two-pass encoders (**Fig. 3**).

5. Application to IP retransmission services

Transcoder equipment using SARA can be used for IP retransmission (retransmission of digital TV programs over an Internet protocol network) services on the Next Generation Network (NGN). In Japan, it is now being applied to retransmission of digital terres-



TRISC: top-level RISC
VIF: video interface
IR: image reduction
MBP: macroblock-based preprocess
RIT: recording information transform
MRISC: M-CORE RISC
TME: two-pel motion estimation
FME: full-pel motion estimation
SME: sub-pel motion estimation
IPD: intra prediction
TQ: transformation and quantization
CRISC: C-CORE RISC
EC: entropy coding
LF: loop filter
MUX: multiplexer
MDT: multichip data transfer
MIF: memory interface
eDRAM: embedded DRAM

Fig. 2. SARA coding architecture.

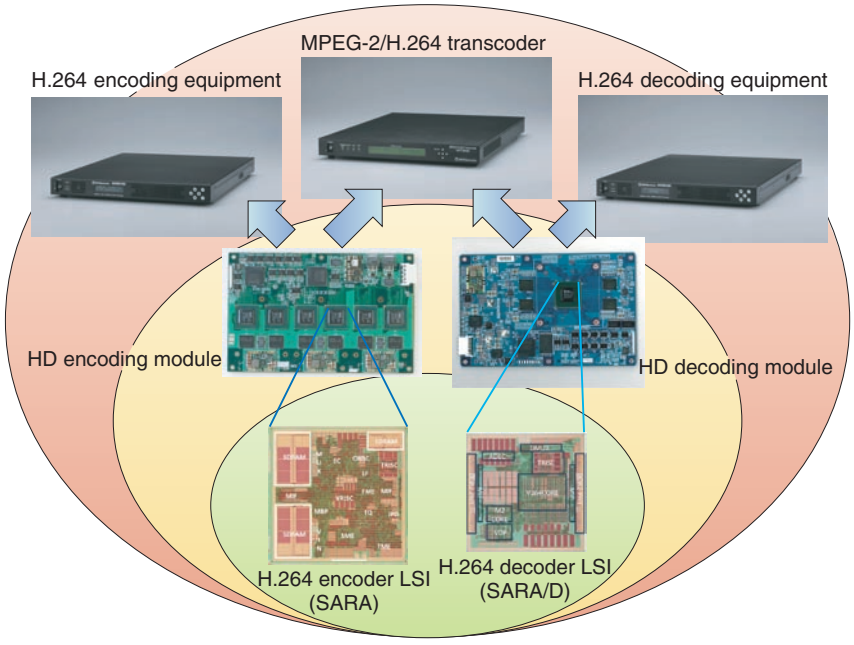


Fig. 3. SARA LSIs, HD encoding/decoding modules, and codec equipment.

trial broadcasts and will soon be used for retransmission of digital BS broadcasting (BS: broadcasting satellite). In the service launched in May 2008, MPEG-2 HD video of digital terrestrial broadcasts encoded at about 14 Mbit/s is converted to H.264 video at 9 Mbit/s while image quality is maintained. This level of compression enables multichannel viewing.

Before this service could be launched, strict guidelines for delay and image quality had to be satisfied in order to obtain approval for retransmission from the broadcast studios involved. Our transcoder was recognized as the first codec equipment in the world to satisfy these guidelines, and it was chosen for use in the Tokyo and Osaka areas. The plan is to deploy this transcoder in steps as the IP retransmission service expands throughout Japan. The SARA LSI is destined to be a key device in video codec equipment for professional broadcasting use.

References

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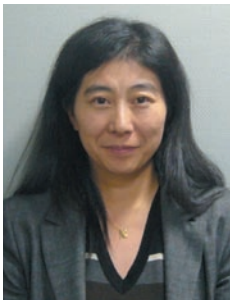
Koyo Nitta
Senior Research Engineer, NTT Cyber Space Laboratories.
He received the B.E. and M.E. degrees in information science from Kyoto University in 1993 and 1995, respectively. He joined NTT LSI Laboratories in 1995 and engaged in R&D of parallel signal processing.



Hiroe Iwasaki
Senior Research Engineer, NTT Cyber Space Laboratories.
She received the B.S. and Ph.D. degrees in information science from Tsukuba University, Ibaraki, in 1992 and 2006, respectively. She joined NTT Switching System Laboratories in 1992. She has been engaged in R&D of an architecture and realtime operating system for multimedia embedded system LSIs. She moved to NTT Cyber Space Laboratories in 1997. She is a member of IEEE, the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan, and the Information Processing Society of Japan (IPSJ).

Jiro Naganuma
Senior Marketing Engineer, Business Strategy Office, Digital Video Business Group, NTT Electronics Corporation.
He received the B.S. degree in electrical engineering from Tokushima University and the Ph.D. degree in information science from Kyoto University in 1981 and 1995, respectively. He joined the Musashino Electrical Communication Laboratories of Nippon Telegraph and Telephone Public Corporation (now NTT) in 1981. He engaged in R&D of high-level architectures and design methodologies for multimedia system LSIs, in particular, MPEG-2 codec LSIs (VASA and ISIL) and H.264 codec LSIs (SARA), their codec systems, and their applications. He received the President's Award from NTT in 1996, 2001, and 2004, the 33rd Japan Industrial Technology Award (Prime Minister's Award) from Nikkan Kogyo Shimbun in 2005 (for NTT Corporation), the 51st Maejima Award from the Teishin Association in 2006, and the Prize for Science and Technology (Development Category) from the Minister of Education, Culture, Sports, Science and Technology in 2007. He is a member of IEICE and IPSJ. At the time of the research reported here, he was Senior Research Engineer, Supervisor, Visual Media Communications Project, Director of Promotion Project 1, NTT Cyber Space Laboratories. He moved to NTT Electronics in 2009.