Letters

High-speed, High-reliability 0.5-µm-emitter InP-based Heterojunction Bipolar Transistors

Norihide Kashio[†], Kenji Kurishima, Yoshino K. Fukai, and Shoji Yamahata

Abstract

We have developed 0.5- μ m-emitter InP heterojunction bipolar transistors (HBTs) towards over-100-Gbit/s integrated circuit applications. The HBTs incorporate a passivation ledge structure and tungstenbased emitter metal to achieve high reliability at a high collector current density. The fabricated HBT exhibits a current gain of 58, f_t of 321 GHz, and f_{max} of 301 GHz at a collector current density of 4 mA/ μ m². The results of accelerated life tests predict an activation energy of around 1.5 eV and the extrapolated mean time to failure is over 10⁸ hours at a junction temperature of 125°C.

1. Introduction

The remarkable high-speed performance and high breakdown voltages of InP-based heterojunction bipolar transistors (HBTs) make them promising candidates for use in ultrahigh-speed integrated circuits (ICs) for future optical fiber communications systems [1]. Several ICs operating at over 100 Gbit/s have already been demonstrated using InP HBTs [2]. However, for such InP HBTs to be used in practical applications, they must have excellent reliability.

Some reliability data for InP HBTs has been reported in recent years [3]. In InP HBTs, degradation, such as current gain degradation, is primarily caused by surface recombination at the emitter-base periphery. An effective way to suppress the recombination current is to use a ledge structure on an external base layer [4]. Indeed, we have achieved excellent reliability in InP HBTs with a passivation ledge structure for 40-Gbit/s IC applications [5]. Our baseline HBT consists of a 300-nm-thick InGaAs collector, 50-nmthick base, and 70-nm-thick InP emitter. The ledge structure was fabricated using the emitter layer on the external base. For the ledge layer, undoped InP is suitable because it can be easily depleted. It is also effective in reducing the emitter-base capacitance, which is advantageous for low-power operation [6]. An HBT with a 1 μ m × 4 μ m emitter exhibits currentgain cut-off frequency f_t of 169 GHz, maximum oscillation frequency f_{max} of 255 GHz, and current gain of 57 at a collector current density J_c of 1 mA/ μ m². The extrapolated mean time to failure (MTTF) is estimated to be over 1 × 10⁸ hours at a junction temperature T_j of 125°C, and the degradation does not depend on J_c up to 2 mA/ μ m².

To build over-100-Gbit/s ICs, we need f_t and f_{max} to be over 300 GHz. High J_c (> 2 mA/µm²) is essential to achieve these values. However, at such high- J_c operation, a sudden degradation in current gain frequently occurs [5] because of diffusion of the emitter metal, which consists of Ti/Pt/Au. Under thermal stress, Ti diffuses into the emitter, which reduces the barrier effect of Ti. Then, Au diffuses into the emitter and base, which results in sudden breakdown in the emitter-base junction.

This article describes highly reliable submicrometer InP HBTs toward over-100-Gbit/s IC applications. To achieve excellent reliability at high J_c , we used tungsten-based emitter metal as well as passivation

[†] NTT Photonics Laboratories

Atsugi-shi, 243-0198 Japan



Fig. 1. Cross-sectional view of an InP HBT with the passivation ledge structure and tungsten-based emitter metal.



Fig. 2. Common-emitter collector *I-V* characteristics for a fabricated HBT with a 0.5 μ m × 3.0 μ m emitter.

ledge structures. Here, the tungsten-based emitter metal acts as a barrier to Ti and Au. The HBT structures were laterally and vertically scaled down to provide higher f_t . Section 2 explains the HBT structures and fabrication. Section 3 discusses the effectiveness of the passivation ledge structure and the high-frequency performance and presents the results of accelerated life tests, which indicate that the HBTs have excellent reliability even at $J_c = 7 \text{ mA}/\mu\text{m}^2$.

2. HBT structures and fabrication

A cross-sectional view of the fabricated InP HBT is shown in **Fig. 1**. A single HBT structure was grown on a 3-inch InP substrate by molecular beam epitaxy. The epitaxial layers were vertically scaled down to halve the carrier transit time. The base and collector layers were 35-nm-thick lattice-matched p-InGaAs and 150-nm-thick InGaAs, respectively. The base layer was doped with carbon to a concentration of 5 $\times 10^{19}$ cm⁻³. The base sheet resistance was estimated to be 646 Ω /sq. by transmission line mode measurements. The emitter was 50-nm-thick n-InP. The emitter doping level was optimized to provide high J_c and high current gain [7]. In addition to the vertical scaling, the emitter width was scaled down to 0.5 µm to reduce the base-collector capacitance and collector current. The device fabrication sequence was the same as that for our baseline HBTs [5], except for the deposition of tungsten-based emitter metal to prevent Ti/Au diffusion. First, tungsten-based emitter metals were deposited, followed by photoresist mask. Next, dry etching was performed to remove the emitter metal and about half of the emitter layer. The remaining emitter layer was used as a ledge layer. The ledge thickness was about 30 nm. The surface of the ledge layer was covered with SiN film for passivation. Then, base metal was formed in a non-self-aligned manner. For the device layout, a base-pad isolation structure was used to eliminate the extrinsic base-collector capacitance at the base-pad area [8]. Finally, the devices were isolated by wet etching and passivated with benzocyclobutene.

3. Device characterization

3.1 DC characteristics

Typical *I-V* characteristics for the fabricated HBT are shown in **Fig. 2**. The emitter was 0.5 μ m wide and 3 μ m long. The HBT exhibited excellent turn-on characteristics and high current density of over 10 mA/ μ m². The breakdown voltage was over 3 V.

A Gummel plot for the HBT at a collector-emitter voltage V_{CE} of 1.2 V is shown in **Fig. 3**. Even at a low J_c , there is no crossover in the Gummel plot. The dc



Fig. 3. Common-emitter collector *I-V* characteristics for the fabricated HBT with a 0.5 μ m × 3.0 μ m emitter.



Fig. 4. Dependence of current gain on collector current density for four HBTs with different emitter sizes.

current gain β was 58 at $J_c = 4 \text{ mA}/\mu\text{m}^2$, which is a reasonably high value. The ideality factors of the collector and base currents were 1.3 and 1.6, respectively. To investigate the effectiveness of the passivation ledge layers, we measured Gummel plots of HBTs with different emitter areas. The J_c dependence of β for HBTs with different emitter sizes is shown in **Fig. 4**. We used a collector-base voltage V_{CB} of 0 V to eliminate any influence of impact ionization current



Fig. 5. Periphery recombination current J_L as a function of J_c . For comparison, results for HBTs without the ledge structure [10] are also shown.

at the base-collector junction. At $J_c > 0.1 \text{ mA}/\mu\text{m}^2$, current gain degradation due to emitter size reduction was very small. To obtain more information about the current-gain characteristics, we analyzed the base recombination current using the well-known formula [9]

$$\frac{1}{\beta} = \left(\frac{J_{\rm bi}}{J_{\rm c}}\right) + \frac{J_{\rm L}}{J_{\rm c}} \left(\frac{L_{\rm E}}{S_{\rm E}}\right) \,, \tag{1}$$

where J_{bi} is the recombination current density under the emitter-base internal junction, J_L is the emitter periphery recombination current per unit length, L_E is the emitter periphery length, and S_E is the junction area. J_L is plotted as a function of J_c in **Fig. 5**. The J_L values were obtained from the slope of the dependence of β^{-1} on the periphery-to-area ratio L_E/S_E using Eq. (1). For comparison, results for InP HBTs without a passivation ledge structure [10] are also shown. For the HBTs in this work, the J_L value was only 0.3 $\mu A/\mu m$ at $J_c = 1 \text{ mA}/\mu m^2$, which is one order of magnitude lower than that of the HBTs without a ledge structure. This indicates that the ledge layer is depleted, which suppresses surface recombination at the emitter-base periphery.

3.2 High-frequency characteristics

The high-frequency performance of the fabricated HBTs was characterized by S-parameter measurements from 0.5 to 50 GHz using an HP8510C network analyzer. The S-parameters were de-embedded by subtracting the pad's parasitic capacitance extracted from the measurement of an open pad structure.



Fig. 6. Current gain (h_{21}), Mason's unilateral gain (UG), maximum stable gain (MSG), and stability factor K as functions of frequency at $J_c = 4$ mA/mm² and $V_{CE} = 1.2$ V.



Fig. 7. f_{t} , f_{max} , and C_{Tc} as functions of J_{c} .

The current gain (h_{21}), Mason's unilateral gain (UG), maximum stable gain, and the stability factor are shown in **Fig. 6** as functions of frequency at $J_c = 4$ mA/mm² and $V_{CE} = 1.2$ V. The emitter was 0.5 µm wide and 4 µm long. The f_t and f_{max} were obtained by extrapolating h_{21} and UG for a line with a slope of -20 dB/decade. The f_t , f_{max} , and total collector capacitance C_{Tc} are shown in **Fig. 7** as functions of J_c . The HBT exhibited a peak f_t of 321 GHz and peak f_{max} of



Fig. 8. Sum of emitter charging time $r_e C_e$ and carrier transit time t_F as a function of inverse collector current $1/I_c$.

301 GHz at $J_c = 4 \text{ mA}/\mu\text{m}^2$. Note that C_{Tc} was 6.4 fF. The C_{Tc} value is almost the same as that of our baseline HBTs with a collector thickness of 300 nm [5], [6], which means that the emitter size reduction effectively eliminated the C_{Tc} .

Next, we extracted the carrier transit time τ_F from the measured *S*-parameters of the HBT with a 0.5 µm × 4 µm emitter. On the basis of the HBT small-signal T-model equivalent circuit [11], the sum of τ_F , emitter charging time r_eC_e , and R_cC_{Tc} product is expressed as

$$r_{\rm e}C_{\rm e} + \tau_{\rm F} + R_{\rm c}C_{\rm Tc} = \frac{-1}{\omega} \, {\rm Im} \left[\frac{Z_{12} - Z_{21}}{Z_{22} - Z_{21}} \right] / {\rm Re} \left[\frac{Z_{12} - Z_{21}}{Z_{22} - Z_{21}} \right],$$
(2)

where r_e is the emitter dynamic resistance, C_e is the emitter-base capacitance, and R_c is the collector resistance. The Z-parameters (Z₁₁, Z₁₂, Z₂₁, Z₂₂) were obtained from the measured S-parameters. R_c was estimated from the subcollector sheet resistance and contact resistivity, which were determined by transmission line mode measurements.

The sum of r_eC_e and τ_F as a function of inverse collector current is shown in **Fig. 8**. By extrapolating the fitting line to $1/I_c = 0$, we estimated τ_F to be 0.34 ps, which is half that of our baseline HBTs [5], [10]. This τF value corresponds to an average carrier velocity in the base and collector of 3.2×10^7 cm/s. An effective way to boost the average carrier transit velocity is to



Fig. 9. Changes in normalized current gain β/β_0 of our baseline HBTs at $J_c = 5 \text{ mA}/\mu\text{m}^2$ as a function of stress time.

use a compositionally graded pseudomorphic base. We previously reported an average carrier velocity of 4×10^7 cm/s [12]. Furthermore, the pseudomorphic base is also effective in lowering the base sheet resistance, which is beneficial for obtaining higher f_{max} . To achieve higher f_{t} and f_{max} , we will fabricate HBTs with a pseudomorphic base in the near future.

3.3 Reliability

To investigate the reliability of the newly developed InP HBTs with over-300-GHz f_t , we performed accelerated life tests. For each test, more than ten packaged transistors were used. Each transistor was continuously biased in a high-temperature oven filled with nitrogen. The bias conditions were $V_{CB} = 0$ V and V_{BE} = 0.9–1.0 V, depending on the operating J_c . The ambient temperatures T_a were 165, 175, and 195°C. Initial device characterization and stressed device characterization were performed at room temperature at V_{CE} = 1.2 V using a semiconductor parameter analyzer. Here, the stressed device was cooled to room temperature before the characterization. Junction temperatures T_i of the devices were estimated from the thermal resistance, which was obtained by the method in ref. [13]. In the life tests, we used the newly developed HBT. Its emitter contact metal is tungstenbased metal and its epitaxial layer structure is the same as that for the HBT presented in the previous sections. The emitter was 0.5 μ m wide and 3.0 μ m long. For comparison, we also tested our baseline



Fig. 10. Gummel plots of the newly developed HBT after various stress times. The emitter size was 0.5 μm \times 3 $\mu m.$

HBT with Ti/Pt/Au emitter contact metal for 40-Gbit/s ICs [5], for which the emitter was 1 μ m wide and 4 μ m long. In this section, we first explain the degradation modes of our baseline HBT and then discuss the degradation mechanism of the newly developed HBT.

Changes in normalized dc current gain β/β_0 of our baseline HBTs at $J_c = 5 \text{ mA}/\mu\text{m}^2$ are shown in **Fig. 9** as a function of stress time, where β_0 is the current gain before the reliability test. The stress conditions were $V_{\text{BE}} = 1.0 \text{ V}$ and $V_{\text{CB}} = 0 \text{ V}$, for which J_c was 5 mA/ μ m². T_a was 195°C and T_j was estimated to be 289°C. As we reported previously [5], the degradation of dc current gain has two modes: gradual degradation (mode 1), which is attributed to thermal degradation of the quality at the external base surface between the ledge and the base metal, and sudden degradation caused by Ti/Au diffusion into semiconductors (mode 2).

Gummel plots of the newly developed HBT after the various stress times are shown in **Fig. 10**. The emitter was 0.5 µm wide and 3 µm long. After the HBT was stressed for a particular period of time, it was cooled to room temperature and then the Gummel plots were measured at $V_{CE} = 1.2$ V. To enable us to compare the life test results for the newly developed HBTs with those for the baseline HBTs, the T_j values of both devices should be almost the same because the degradation of dc current gain depends not on T_a but on T_j . The stress conditions were $V_{BE} =$



Fig. 11. Changes in β/β₀ of the newly developed HBTs with stress time. The β/β₀ was obtained from the Gummel plots in Fig. 10.

0.98 V and $V_{\text{CB}} = 0$ V, for which J_c was 7 mA/ μ m². T_a was 165°C, and T_j was estimated to be 284°C. Although the base current gradually increased at low V_{BE} , there was no sudden degradation in the base and collector currents with stress time.

The changes in β/β_0 at $J_c = 7 \text{ mA}/\mu\text{m}^2$ with stress time are shown in **Fig. 11**. The β/β_0 was obtained from the Gummel plots in Fig. 10. Although β/β_0 gradually decreased, no sudden drop in β/β_0 , resulting from mode 2, was observed. This means that the tungsten-based emitter metal firmly suppressed the Ti/Au diffusion. Thus, the degradation of dc current gain in the newly developed HBT was mainly due to mode 1.

Finally, we estimated the activation energy of degradation in the newly developed HBTs. The MTTF in each life test was determined by the median rank method using a Weibull distribution. The failure criterion was a 15% reduction in β/β_0 . Arrhenius plots of β for the baseline HBTs [5] are shown in **Fig. 12**. The MTTFs of the newly developed HBTs are also plotted. The activation energy $\bar{E_a}$ for the baseline \hat{HBTs} was estimated to be 1.5 eV. The newly developed HBTs had a similar MTTF tendency to the baseline HBTs. Thus, their E_a is expected to be around 1.5 eV, and the extrapolated MTTF at $T_i = 125^{\circ}C$ is expected to be over 10^8 hours [14]. On the basis of these results, this submicrometer InP-based HBT technology is promising for making high-reliability ultrahigh-speed ICs.



Fig. 12. Arrhenius plots of MTTF of β for our baseline HBTs [5], where the failure criterion was a 15% reduction in β/β_0 . The MTTF of the newly developed HBTs is also plotted.

References

- [1] W. Snodgrass, W. Hafez, N. Harff, and M. Feng, "Pseudomorphic InP/InGaAs Heterojunction Bipolar Transistors (PHBTs) Experimentally Demonstrating $f_T = 765$ GHz at 25°C Increasing to $f_T = 845$ GHz at -55°C," Tech. Dig. Int. Electron Device Meeting (IEDM'06), pp. 11–13, San Francisco, CA, USA, 2006.
- [2] K. Murata, K. Sano, T. Enoki, H. Sugahara, and M. Tokumitsu, "InP-Based IC Technologies for 100-Gb/s and beyond," Proc. of Indium Phosphide and Related Materials (IPRM'04), pp. 10–15, Kagoshima, Japan, 2004.
- [3] M. Yanagisawa, K. Kotani, T. Kawasaki, R. Yamabi, S. Yaegassi, and H. Yano, "A Robust All-wet-etching Process for Mesa Formation of InGaAs-InP HBT Featuring High Uniformity and High Reproducibility," IEEE Trans. Electron Devices, Vol. 51, No. 8, pp. 1234–1240, 2004.
- [4] E. Tokumitsu, A. G. Dentai, and C. H. Joyner, "Reduction of the Surface Recombination Current in InGaAs/InP Pseudo-Heterojunction Bipolar Transistors Using a Thin InP Passivation Layer," IEEE Electron Devices, Vol. 10, No. 12, pp. 585–587, 1989.
- [5] Y. K. Fukai, K. Kurishima, M. Ida, S. Yamahata, and T. Enoki, "Highly Reliable InP-Based HBTs with a Ledge Structure Operating at High Current Density," Electronics and Communication in Japan, part 2, Vol. 90, No. 4, pp. 1–8, 2007.
- [6] M. Ida, K. Kurishima, H. Nakajima, N. Watanabe, and S. Yamahata, "Undoped-emitter InP/InGaAs HBTs for High-speed and Low-power Applications," Tech. Dig. Int. Electron Device Meeting (IEDM'00), pp. 854–856, San Francisco, CA, USA, 2000.
- [7] N. Kashio, K. Kurishima, Y. K. Fukai, S. Yamahata, and Y. Miyamoto, "Emitter layer design for high-speed InP HBTs with high reliability," Indium Phosphide Related Materials (IPRM'07), pp. 441–442, Matsue, Japan, 2007.
- [8] M. Ida, S. Yamahata, H. Nakajima, and N. Watanabe, "High-performance small InP/InGaAs HBTs with reduced parasitic base-collector capacitance fabricated using a novel base-metal design," Proc. of Int. Symp. on Compound Semiconductors (ISCS), Inst. Phys. Conf. Ser. No. 106, pp. 293–296, Berlin, Germany, 1999.
- [9] K. Kurishima, H. Nakajima, S. Yamahata, T. Kobayashi, and Y. Matsuoka, "Growth, Design and Performance of InP-Based Heterostruc-

ture Bipolar Transistors," IEICE Trans. Electron., Vol. E78-C, No. 9, pp. 1171–1181, 1995.

- [10] H. Nakajima, K. Kurishima, S. Yamahata, T. Kobayashi, and Y. Matsuoka, "Lateral Scaling Investigation on DC and RF Performances of InP/InGaAs Heterojunction Bipolar Transistors," IEICE Trans. Electron., Vol. E78-C, No. 2, pp. 186–192, 1995.
- [11] S. J. Spiegel, D. Ritter, R. A. Hamm, A. Feygenson, and P. R. Smith, "Extraction of the InP/InGaAs Heterojunction Bipolar Transistor Small-Signal Equivalent Circuit," IEEE Trans. Electron Devices, Vol. 42, No. 6, pp. 1059–1064, 1995.
- [12] M. Ida, K. Kurishima, and N. Watanabe, "Ultrahigh-speed InP/ InGaAs DHBTs with Very High Current Density," IEICE Trans. Electron., Vol. E86-C, No. 10, pp. 1923–1928, 2003.
- [13] D. E. Dawson, A. K. Gupta, and M. L. Salib, "CW Measurement of HBT Thermal Resistance," IEEE Electron Devices, Vol. 39, No. 10, pp. 2235–2239, 1992.
- [14] N. Kashio, K. Kurishima, Y. K. Fukai, and S. Yamahata, "Highly Reliable Submicron InP-based HBTs with over 300-GHz ft," IEICE Trans. Electron., Vol. E91-C, No. 7, pp. 1084-1090, 2008.



Norihide Kashio

Research Engineer, Heterostructure Devices Research Group, NTT Photonics Laboratories. He received the B.S. and M.S. degrees in electrical engineering from Waseda University, Tokyo, in 2000 and 2002, respectively. He joined NTT Photonics Laboratories in 2002, where he engaged in research on ultrahigh-speed InPbased optical and electrical devices for future optical fiber communications systems. He is a member of the Institute of Electronics, Information and Communication Engineers of Japan and the Japan Society of Applied Physics (JSAP).



Yoshino K. Fukai

Senior Research Engineer, Heterostructure Devices Research Group, NTT Photonics Laboratories.

She received the M.S. degree in physics and applied physics from Waseda University, Tokyo, in 1986 and joined NTT in 1986. She is currently engaged in research on high-reliability techniques for InP devices.



Kenji Kurishima

Senior Research Engineer, Heterostructure Devices Research Group, NTT Photonics Laboratories.

He received the B.S., M.S., and Dr.Eng. degrees in physical electronics from Tokyo Institute of Technology in 1987, 1989, and 1997, respectively. He joined NTT Atsugi Electrical Communications Laboratories in 1989, where he engaged in R&D of InP-based HBTs and MOVPE growth. His current research interests include the design and fabrication of high-speed electronic devices for future communications systems.



Shoji Yamahata

Group Leader, Heterostructure Devices Research Group, NTT Photonics Laboratories.

He received the B.S. and M.S. degrees in polymer science and the Ph.D. degree in physics from Hokkaido University in 1982, 1984, and 1996, respectively. He joined the Electrical Communications Laboratories of Nippon Telegraph and Telephone Public Corporation (now NTT) in 1984, where he worked on III-V compound semiconductor transistors. Since 1989, he has been engaged in research on GaAs- and InP-based heterojunction transistors at NTT Photonics Laboratories. He is a member of JSAP.