External Awards

Electronics Society Award
Winners: Masahiro Nada, Toshihide Yoshimatsu, NTT Device Innovation Center; Hideaki Matsuzaki, NTT Device Technology Laboratories
Date: March 31, 2021
Organization: The Institute of Electronics, Information and Communication Engineers (IEICE) Electronics Society

For their pioneering research and development of high-speed avalanche photodiodes with a vertical-illumination structure for optical fiber communications.

FIT Encouragement Award
Winner: Yuya Omori, NTT Device Innovation Center
Date: August 27, 2021
Organization: Information Processing Society of Japan (IPSJ)

For "Complexity Reduction Based on Equivalence and Continuity of Convolutional Layers in CNN Inference."
Published as: Y. Omori, D. Kobayashi, S. Yoshida, S. Hatta, H. Uzawa, K. Nakamura, and K. Sano, "Complexity Reduction Based on Equivalence and Continuity of Convolutional Layers in CNN Inference," Proc. of 20th Forum on Information Technology (FIT2021), Vol. 1, pp. 179–180, Aug. 2021.

Best Paper Award (Research track)
Winners: Yukako Iimura and Shinobu Saito, NTT Computer and Data Science Laboratories
Date: September 8, 2021
Organization: IPSJ Special Interest Group on Software Engineering (SIGSE)

For "Practical Report on Software Development Approach for Promoting Workstyle Flexibility."
Published as: Y. Iimura and S. Saito, "Practical Report on Software Development Approach for Promoting Workstyle Flexibility," Proc. of IPSJ/SIGSE Software Engineering Symposium 2021, pp. 14–22, Sept. 2021.

Distinguished Contributions Award
Winner: Doohwan Lee, NTT Network Innovation Laboratories
Date: September 15, 2021
Organization: IEICE Communications Society

For his contributions as a peer reviewer for papers submitted to the IEICE Communications Society.

Young Scientist Presentation Award
Winner: Koji Sakai, NTT Basic Research Laboratories
Date: September 21, 2021
Organization: The Japan Society of Applied Physics (JSAP)

For "Development of 3D-cultured Neuronal Network in Graphene-based Self-folding Electrode Array."
Published as: K. Sakai, T. Teshima, T. Goto, H. Nakashima, and M. Yamaguchi, "Development of 3D-cultured Neuronal Network in Graphene-based Self-folding Electrode Array," The 68th JSAP Spring Meeting 2021, Mar. 2021.

Young Scientist Presentation Award
Winner: Ai Ikeda, NTT Basic Research Laboratories
Date: September 21, 2021
Organization: JSAP

For "Novel Superconducting $(CaCuO_2)_n/(Ca_2Fe_2O_5)_m$ Superlattices Prepared by MBE."
Published as: A. Ikeda, Y. Krockenberger, Y. Taniyasu, and H. Yamamoto, "Novel Superconducting $(CaCuO_2)_n/(Ca_2Fe_2O_5)_m$ Superlattices Prepared by MBE," The 68th JSAP Spring Meeting 2021, Mar. 2021.

Young Scientist Presentation Award
Winner: Takahiro Kashiwazaki, NTT Device Technology Laboratories
Date: September 21, 2021
Organization: JSAP

For "Terahertz-order Broadband Measurement of Squeezed Light by Optical Parametric Amplification for Ultra-fast Optical Quantum Computing."
Published as: T. Kashiwazaki, N. Takanashi, A. Inoue, T. Kazama, K. Enbutsu, R. Kasahara, T. Umeki, and A. Furusawa, "Terahertz-order Broadband Measurement of Squeezed Light by Optical Parametric Amplification for Ultra-fast Optical Quantum Computing," The 68th JSAP Spring Meeting 2021, Mar. 2021.

Young Scientist Presentation Award
Winner: Takuma Tsurugaya, NTT Device Technology Laboratories
Date: September 21, 2021
Organization: JSAP

For "Photonic Reservoir Computing Using Low-power-consumption SOA."
Published as: T. Tsurugaya, T. Hiraki, M. Nakajima, T. Aihara, N.-P. Diamantopoulos, T. Fujii, T. Segawa, and S. Matsuo, "Photonic Reservoir Computing Using Low-power-consumption SOA," The 68th JSAP Spring Meeting 2021, Mar. 2021.

Papers Published in Technical Journals and Conference Proceedings

Divide-and-conquer Verification Method for Noisy Intermediate-scale Quantum Computation

Y. Takeuchi, Y. Takahashi, T. Morimae, and S. Tani

arXiv:2109.14928, Oct. 2021.

Several noisy intermediate-scale quantum computations can be regarded as logarithmic-depth quantum circuits on a sparse quantum computing chip, where two-qubit gates can be directly applied on only some pairs of qubits. In this paper, we propose a method to efficiently verify such noisy intermediate-scale quantum computation. To this end, we first characterize small-scale quantum operations with respect to the diamond norm. Then by using these characterized quantum operations, we estimate the fidelity $\langle\psi_t|\hat{\rho}_{out}|\psi_t\rangle$ between an actual n-qubit output state $\hat{\rho}_{out}$ obtained from the noisy intermediate-scale quantum computation and the ideal output state (i.e., the target state) $|\psi_t\rangle$. Although the direct fidelity estimation method requires $O(2^n)$ copies of $\hat{\rho}_{out}$ on average, our method requires only $O(D^3\,2^{12D})$ copies even in the worst case, where D is the denseness of $|\psi_t\rangle$. For logarithmic-depth quantum circuits on a sparse chip, D is at most $O(\log n)$, and thus $O(D^3\,2^{12D})$ is a polynomial in n.